# EXOSTIV Using the AC701 Artix-7 evaluation kit

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## **Table of Contents**

E)	(OSTIV – using the AC701 kit	3
	Introduction	3
	Using EXOSTIV with the AC701 evaluation kit	3
	AC701 : overview	3
	Connecting the AC701	4
	Reviewing the .epf files settings for the link configuration	5
	Reviewing the .epf files settings for the capture configuration	5

## References

## **Revision History**

Revision	Modifications
1.0.0	Initial revision
1.0.1	Minor corrections



## EXOSTIV – using the AC701 kit

## Introduction

This document provides information about using EXOSTIV with the AC701 Artix-7 evaluation kit (<u>https://www.xilinx.com/products/boards-and-kits/ek-a7-ac701-g.html</u>).

## Using EXOSTIV with the AC701 evaluation kit

EXOSTIV can be connected to the AC701 evaluation kit through the SFP / SFP+ connector with direct SFP cables or through another connector (e.g. the FMC HPC or FMC LPC connectors), possibly with an adapter.

In this document, we'll describe how to use EXOSTIV with the AC701 FMC HPC connectors, (using the FMC to HDMI adapter of Exostiv Labs (<u>http://www.exostivlabs.com/exostiv/hdmi-to-fmc-module-adapter/</u>)). We provide one .epf file to be used with the EXOSTIV Dashboard, pre-configured for use with this port.





#### **Connecting the AC701**



Set the clock oscillator of the FMC to HDMI module to 125 MHz (see picture below) to match to provided example clock setting. Then, plug the FMC to HDMI module in the AC701 FMC HPC port. Finally plug the HDMI cable provided with the EXOSTIV Probe in the EXOSTIV Probe HDMI connector on one end and in the FMC module HDMI connector on the other end (see pictures below).





### Reviewing the .epf files settings for the link configuration

Using the FMC to HDMI module adapter and the HDMI cable.

#### 'TestAC701-1.7.6-HDMI2ch.epf' or TestAC701-1.8.2-HDMI2ch.epf:

EXOSTIV Dashboard for Xilinx - D:/Projects/Xplorer/Product/Support/X	ilinxEvalKits/AC701/Tests/AC701_Tests/HDMI/2016.4-Projec — 🛛 🗙
Artix-7 part mounted on the AC701 board	We use the HDMI connector type on the EXOSTIV Probe.
Configuration	Insert Debug   EXOSTIV IP Design
FPGA Type Connector Family Artix-7 Connector ty	/pe HDMI
Package fbg676   Speed grade -2   Part xc7a200tfbg676-2	rom the AC701 FMC HPC connector, we select the 2 ransceivers connected to bank 213 of the FPGA (refer
Upstream Link Downstr	o the AC701 documentation to check this onfiguration).
MGT type GTP   MGT_TxP0 AC10   MGT_TxP1 AE9   MGT_TxP2 AC8   MGT_TxP3 AE7	Pin   D18     When using the HDMI connector of EXOSTIV Probe,     we need 2 extra pins for the downstream channel.     These pins from the HDMI connector are mapped     onto the LA00_P_CC and LA00_N_CC pins of the     FMC connector (see: FMC to HDMI module user's     guide).     guide).     These pins of the FPGA on the AC701 – and are of     LVCMOS25 standard.
MGT_REFCLK_P0   AA13     MGT_REFCLK_P1   AA11     Frequency (MHz)   125     Range : 60 MHz to 660 MHz   conn     Line rate (Gb/s)   6.25     Link rate (Gb/s)   12.5     PLL type used   QPLL     EXOSTIV dock output   is 12.5	5 MHz reference clock is generated from the FMC DMI module mounted oscillator. This clock source rovided to the FPGA through the FMC HPC ector and goes to pin AA13 the FPGA (refer to the D1 documentation). From this clock at 125 MHz, an select a line rate of 6.25 Gbps per transceiver. ided that we use 2 transceivers, the total link rate .5 Gbps.
Info : Info : License is activated, expiration : 2020-01-01 00:00:00 Info : Project file "D:/Projects/Xplorer/Product/Support/XilinxEvalKits/AC701/Tests/ Netlist flow Vivado link X EXOSTIV Probe X FPGA link X	AC701_Tests/HDMI/2016.4-Project/TestAC701-1.7.6-HDMI2ch.epf" loaded successfully.



#### Reviewing the .epf files settings for the capture configuration

Please open the .epf files and review them through the EXOSTIV Dashboard interface.

Here are the main characteristics of the example:

0

- There are 5 data generators in the example design. There are connected to 2 capture units:
  - 'Pattern Capture Unit' (16 bits):
    - Digital sine wave: 'Sine' data group
    - A counter: 'Cnt' data group
    - A pseudo random number generator: 'Rnd' data group
    - 'Video Capture Unit' (46 bits):
      - Video (SDI) stream : 'HD-SDI' data group
      - Sine wave with noise : 'NoisySine'.

EXOSTIV Dashboard for Xilinx - D:/Projects/Xp	lorer/Product/Support/Xilinx	EvalKits/AC701/Tests/AC701_T	ests/HDMI/2016.4-	Project/TestAC701-1.7.6	-HDMI2 —				
🕼 🛤 🖬 📓 🗞 💥									
Link Configuration	Capture Configuration	>>>	Insert EXOSTIV IP	<u>&gt;&gt;&gt;</u>	Debug Design				
Capture units (2 out of max. 16)			Pattern						
✓ Pattern	Triggering			Data					
Sine	Trigger unit type	Levels / Edges / Comparisons	<b>•</b>	Fifo depth	1024	-			
Cnt	Bit operations	X, 0, 1, R, F, B, N		Number of data groups	3 out of max, 16				
Rnd	Bus operations	==, >, <, >=, <=, <>, in ra	nge, out of range	Number of data groups	16 out of max 2049				
Double click to add Data Group	Counter width	Disabled	~	Number of data probes	10 OUL OF MAX. 2040				
Video	Sequencer Depth	Disabled	~						
HD-SDI	Storage qualification								
NoisySine	Number of pipes	Disabled	•						
Double click to add Data Group	Sampling Clark								
Double click to add Capture Unit	Sampling Clock								
	u_demo/Clk								
	:								
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Info : Info : License is activated, expiration : 2020-01-01-00 (	0.0					^			
unio : ucense is acuivaleu, expiration : 2020-01-01-0000000 Info : Info : Project file "Dr/Projects/Noncer/Product/Support/NilmyEvalKite/AC701/Tests/AC701 Tests/HDMT/2016 4-Project/TestAC701-1 7 6-HDMT2ch and successfully									
				interrept louded successi		~			
etlist flow   Vivado link 🕱   EXOSTIV Probe 🕱   FPGA link 🕱									



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