

**EXOSTIV**

# **Using the KC705 Kintex-7 evaluation kit**

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## References

## Revision History

Revision	Modifications
1.0.0	<ul style="list-style-type: none"><li>Initial revision</li></ul>
1.0.1	<ul style="list-style-type: none"><li>Corrected minor typos</li></ul>
1.0.2	<ul style="list-style-type: none"><li>Updated with EXOSTIV Dashboard 1.8.2 release</li></ul>
1.0.3	<ul style="list-style-type: none"><li>Updated with EXOSTIV Dashboard 1.8.4 release</li></ul>

# EXOSTIV – using the KC705 kit

## Introduction

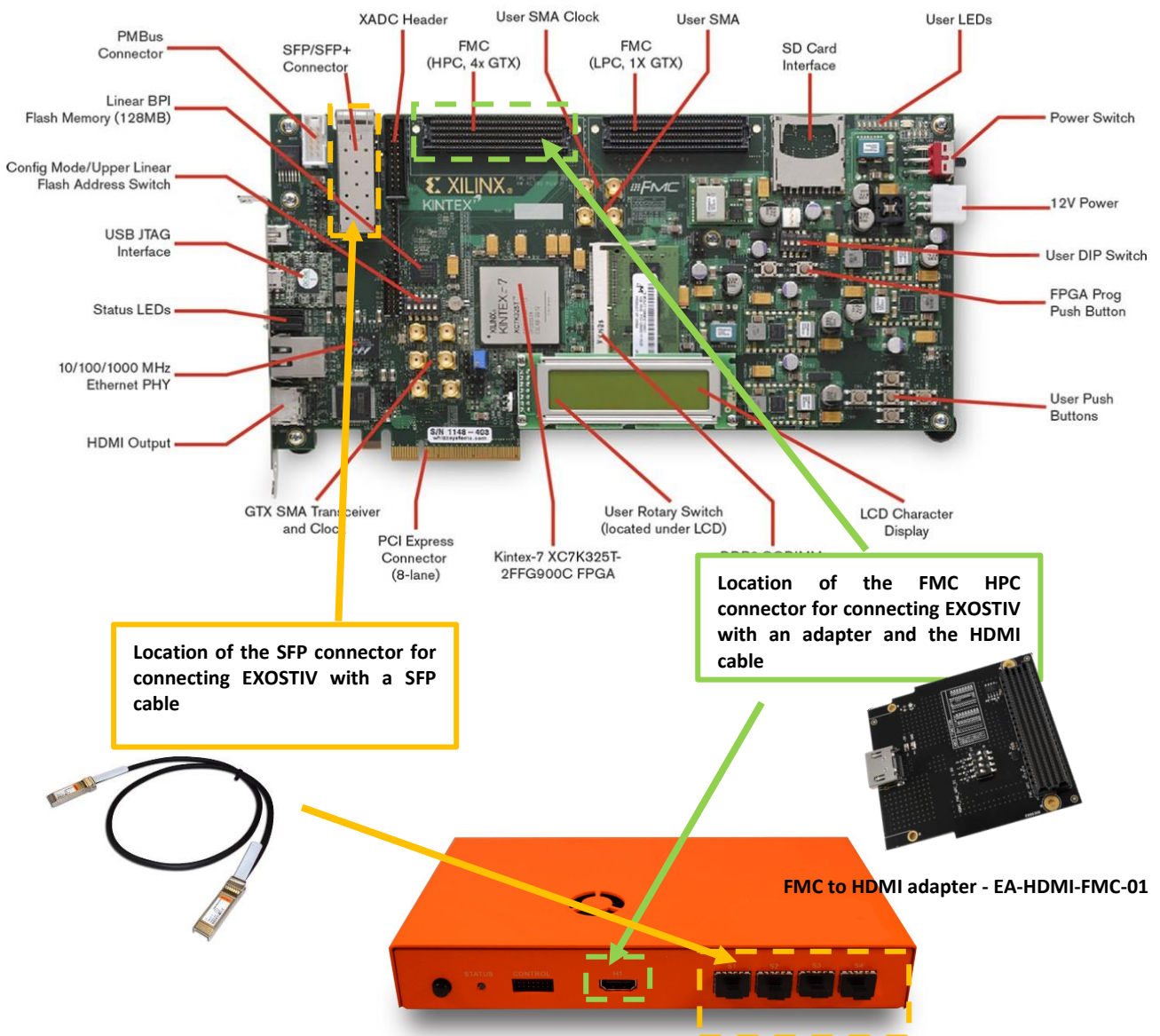
This document provides information about using EXOSTIV with the KC705 Kintex-7 evaluation kit (<https://www.xilinx.com/products/boards-and-kits/ek-k7-kc705-g.html>).

## Using EXOSTIV with the KC705 evaluation kit

EXOSTIV can be connected to the KC705 evaluation kit through the SFP / SFP+ connector with direct SFP cables or through another connector (e.g. the FMC HPC or FMC LPC connectors), possibly with an adapter.

In this document, we'll describe how to use EXOSTIV with the KC705 kit SFP/SFP+ connector and with one of the FMC HPC connectors, with the FMC to HDMI adapter of Exostiv Labs (<http://www.exostivlabs.com/exostiv/hdmi-to-fmc-module-adapter/>). We provide several .epf files to be used with the EXOSTIV Dashboard, that are pre-configured for use with these ports.

### KC705 : overview



## Reviewing the .epf files settings for the link configuration

### Option1: using the SFP connection and on-board SGMII\_CLK for the transceivers

Using a single SFP Cable: simply plug the SFP cable in the KC705 SFP/SFP+ connector and the other end into any of the EXOSTIV Probe SFP ports. The cable used should be able to provide at least 6.25 Gbps bandwidth with the example project standard settings.



'TestKC705-1.8.4-SFP-6G-SGMIIClk.epf':

Kintex-7 part mounted on the KC705 board

The screenshot shows the 'Link Configuration' window in Vivado. The window is titled 'Link Configuration' and has several tabs: 'Link Configuration', 'Capture Configuration', 'Insert EXOSTIV IP', and 'Debug Design'. The 'Link Configuration' tab is active. The window is divided into several sections:

- FPGA Type:** Family: Kintex-7, Package: ffg900, Speed grade: -2, Part: xc7k325tffg900-2.
- Connector:** Connector type: SFP.
- Upstream Link:** Transceiver bank: 117, MGT type: GTX, MGT\_TxP0: K2, MGT\_TxP1: J4, MGT\_TxP2: H2 (checked), MGT\_TxP3: F2.
- Downstream Link:** Use I2C link: , Use transceiver link: , Transceiver bank: 117, MGT\_RxP0: K6, MGT\_RxP1: H6, MGT\_RxP2: G4 (checked), MGT\_RxP3: F6.
- Reference Clock:** Transceiver bank: 117, MGT\_REFCLK\_P0: G8 (checked), MGT\_REFCLK\_P1: J8, Frequency (MHz): 125 (Range: 60 MHz to 670 MHz), Line rate (Gb/s): 6.25, Link rate (Gb/s): 6.25, PLL type used: CPLL, EXOSTIV clock output: .

Red arrows point from text boxes to the following settings:

- From the top-left text box to the 'FPGA Type' section.
- From the top-right text box to the 'Connector type' dropdown.
- From the middle-right text box to the 'MGT\_TxP2' and 'MGT\_RxP2' checkboxes.
- From the bottom-right text box to the 'Frequency (MHz)' and 'Line rate (Gb/s)' dropdowns.

At the bottom of the window, there is a 'Log Window' showing the following messages:

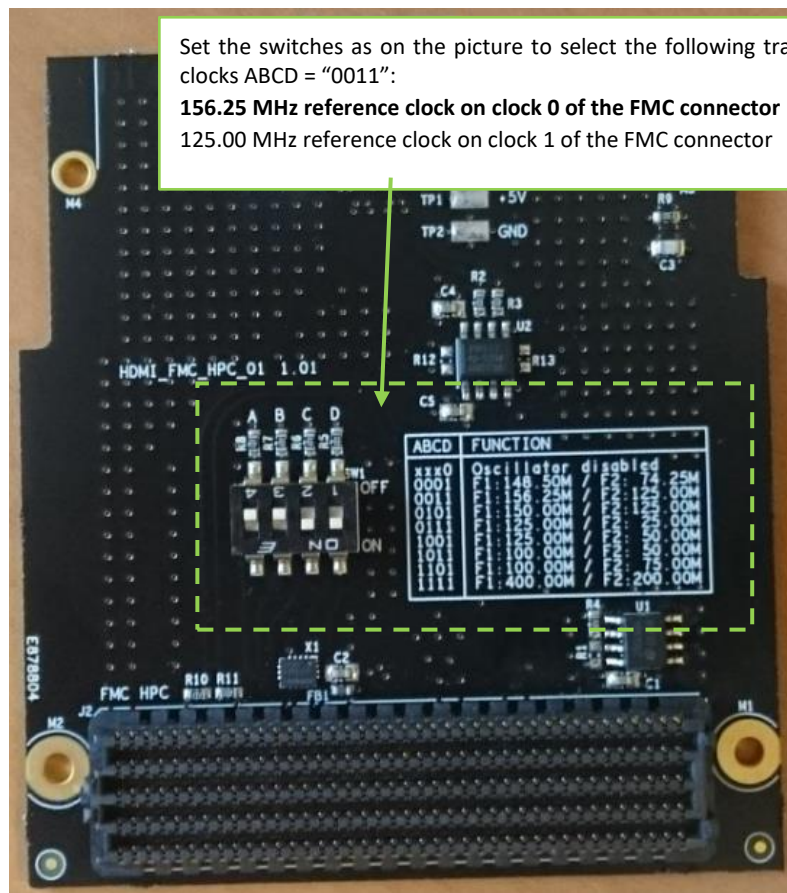
```

Info :
Info : License is activated, expiration : 2020-12-31 00:00:00
Info :
Info : Project file 'D:/Projects/Xplorer/Product/Support/XilinxEvalKits/KC705/KC705_Tests/SFP/Project-Dashboard-1.8.4/TestKC705-1.8.4-SFP-6G.epf' loaded successfully.
Info : Project file 'D:/Projects/Xplorer/Product/Support/XilinxEvalKits/KC705/KC705_Tests/HDMI/Project-Dashboard-1.8.4/TestKC705-1.8.4-HDMI4ch.epf' loaded successfully.
Info : Project file 'D:/Projects/Xplorer/Product/Support/XilinxEvalKits/KC705/KC705_Tests/SFP/Project-Dashboard-1.8.4/TestKC705-1.8.4-SFP-10G.epf' loaded successfully.
Info : Project file 'D:/Projects/Xplorer/Product/Support/XilinxEvalKits/KC705/KC705_Tests/SFP/Project-Dashboard-1.8.4/TestKC705-1.8.4-SFP-6G-SGMIIClk.epf' loaded successfully.
  
```

At the bottom of the window, there are status indicators for 'Netlist flow', 'Vivado link', 'EXOSTIV Probe', and 'FPGA link', all of which are marked with a red 'X'.

**Option 2: using the SFP connection the FMC adapter to generate the reference clock**

The following option allows to reach data rates of 10 Gbps because the clock reference provided from the FMC adapter is of better quality than the KC705 SGMII CLK. This option requires using the FMC plug-in adapter on one of the FMC connectors to supply a clean reference clock at 156.25 MHz and the SFP connector for the data – see picture below.



'TestKC705-1.8.4-SFP-10G.epf':

We use the SFP connector type on the EXOSTIV Probe.

We use SFP2 on the KC705 board. The Tx and Rx P pins of the SFP2 are connected to H2 and G4 pins respectively (bank 117)

A 156.25 MHz reference clock is supplied on the KC705 FMC connector from the connected FMC adapter. This reference clock enters bank 118 at pin C8. With this reference clock, we are able to configure the GTX at 10 Gbps (this example must be used with EP12000 Probe or faster).

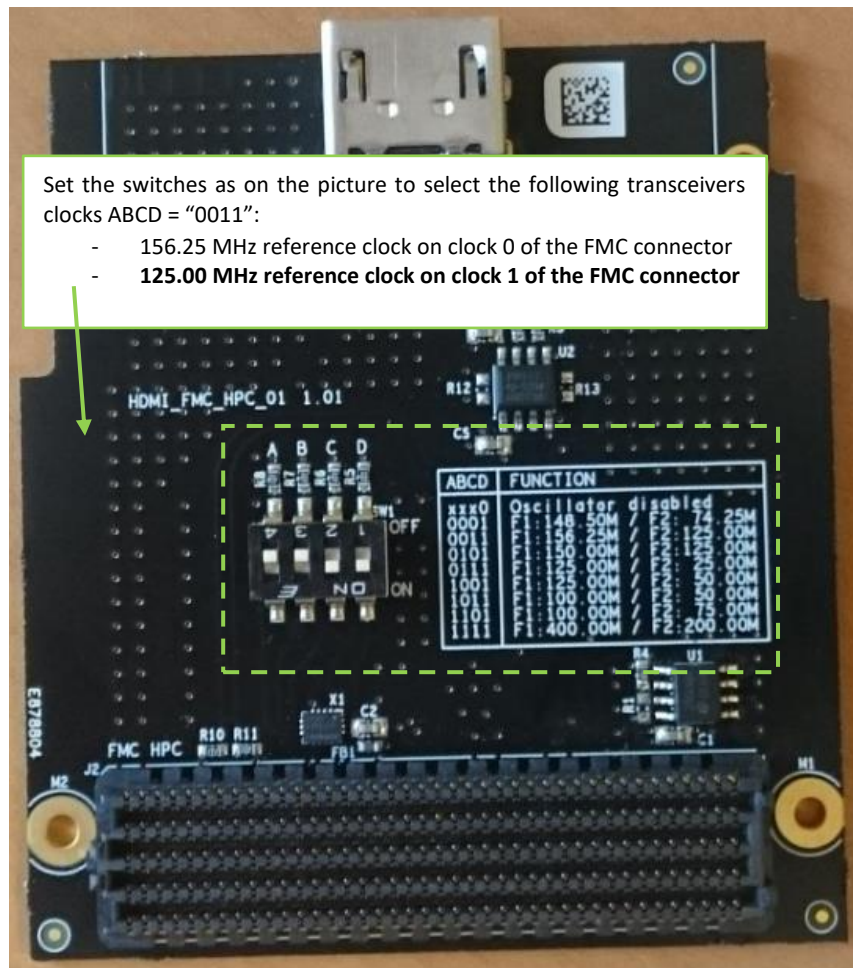
The screenshot shows the EXOSTIV Dashboard for Xilinx configuration window. The 'Link Configuration' tab is active, displaying various settings for the FPGA and transceiver link. The 'FPGA Type' section shows Family: Kintex-7, Package: ffg900, Speed grade: -2, and Part: xc7k325tffg900-2. The 'Connector' section shows Connector type: SFP. The 'Upstream Link' section shows Transceiver bank: 117, MGT type: GTX, and MGT\_TxP2: H2. The 'Downstream Link' section shows Transceiver bank: 117, MGT\_RxP2: G4. The 'Reference Clock' section shows Transceiver bank: 118, MGT\_REFCLK\_P0: C8, Frequency (MHz): 156.25, Line rate (Gb/s): 10, and Link rate (Gb/s): 10. The 'Log Window' at the bottom shows the following messages:

```

Info : Welcome to EXOSTIV Dashboard for Xilinx v1.8.4
Info :
Info : License is activated, expiration : 2020-12-31 00:00:00
Info :
Info : Project file 'D:/Projects/Xplorer/Product/Support/XilinxEvalKits/KC705/KC705_Tests/SFP/Project-Dashboard-1.8.4/TestKC705-1.8.4-SFP-6G.epf' loaded successfully.
Info : Project file 'D:/Projects/Xplorer/Product/Support/XilinxEvalKits/KC705/KC705_Tests/HDMI/Project-Dashboard-1.8.4/TestKC705-1.8.4-HDMI4ch.epf' loaded successfully.
Info : Project file 'D:/Projects/Xplorer/Product/Support/XilinxEvalKits/KC705/KC705_Tests/SFP/Project-Dashboard-1.8.4/TestKC705-1.8.4-SFP-10G.epf' loaded successfully.
  
```

**Option 3: using the FMC to HDMI module adapter and the HDMI cable.**

Set the clock oscillator of the FMC to HDMI module to 156.25 MHz / 125.00 MHz (see picture below) to match to provided example clock setting. Then, plug the FMC to HDMI module in the KC705 FMC HPC port. Finally plug the HDMI cable provided with the EXOSTIV Probe in the EXOSTIV Probe HDMI connector on one end and in the FMC module HDMI connector on the other end (see pictures below).





'TestKC705-1.8.4-HDMI4ch.epf'

Kintex-7 part mounted on the KC705 board

We use the HDMI connector type on the EXOSTIV Probe.

From the KC705 HPC connector, we select all 4 transceivers connected to bank 118 of the FPGA (refer to the KC705 documentation to check this configuration).

When using the HDMI connector of EXOSTIV Probe, we need 2 extra pins for the downstream channel. These pins from the HDMI connector are mapped onto the LA00\_P\_CC and LA00\_N\_CC pins of the FMC connector (see: [FMC to HDMI module user's guide](#)). These pins are connected to the C25 and B25 pins of the FPGA on the KC705 – and are of LVCMOS25 standard.

A 125 MHz reference clock is generated from the FMC to HDMI module mounted oscillator. This clock source is provided to the FPGA through the FMC HPC connector and goes to pin E8 of the FPGA (refer to the KC705 documentation). From this clock at 125 MHz (clock 1 on the FMC adapter), we are able to select a line rate of 6.25 Gbps per transceiver. Provided that we use 4 transceivers, the total link rate is 25 Gbps.

Logging  
Info : Welcome to EXOSTIV Dashboard for Xilinx v1.8.4  
Info :  
Info : License is activated, expiration : 2020-12-31 00:00:00  
Info :  
Info : Project file 'D:/Projects/Xplorer/Product/Support/XilinxEvalKits/KC705/KC705\_Tests/HDMI/Project-Dashboard-1.8.4/TestKC705-1.8.4-HDMI4ch.epf'  
Info : Project file 'D:/Projects/Xplorer/Product/Support/XilinxEvalKits/KC705/KC705\_Tests/HDMI/Project-Dashboard-1.8.4/TestKC705-1.8.4-HDMI4ch.epf'

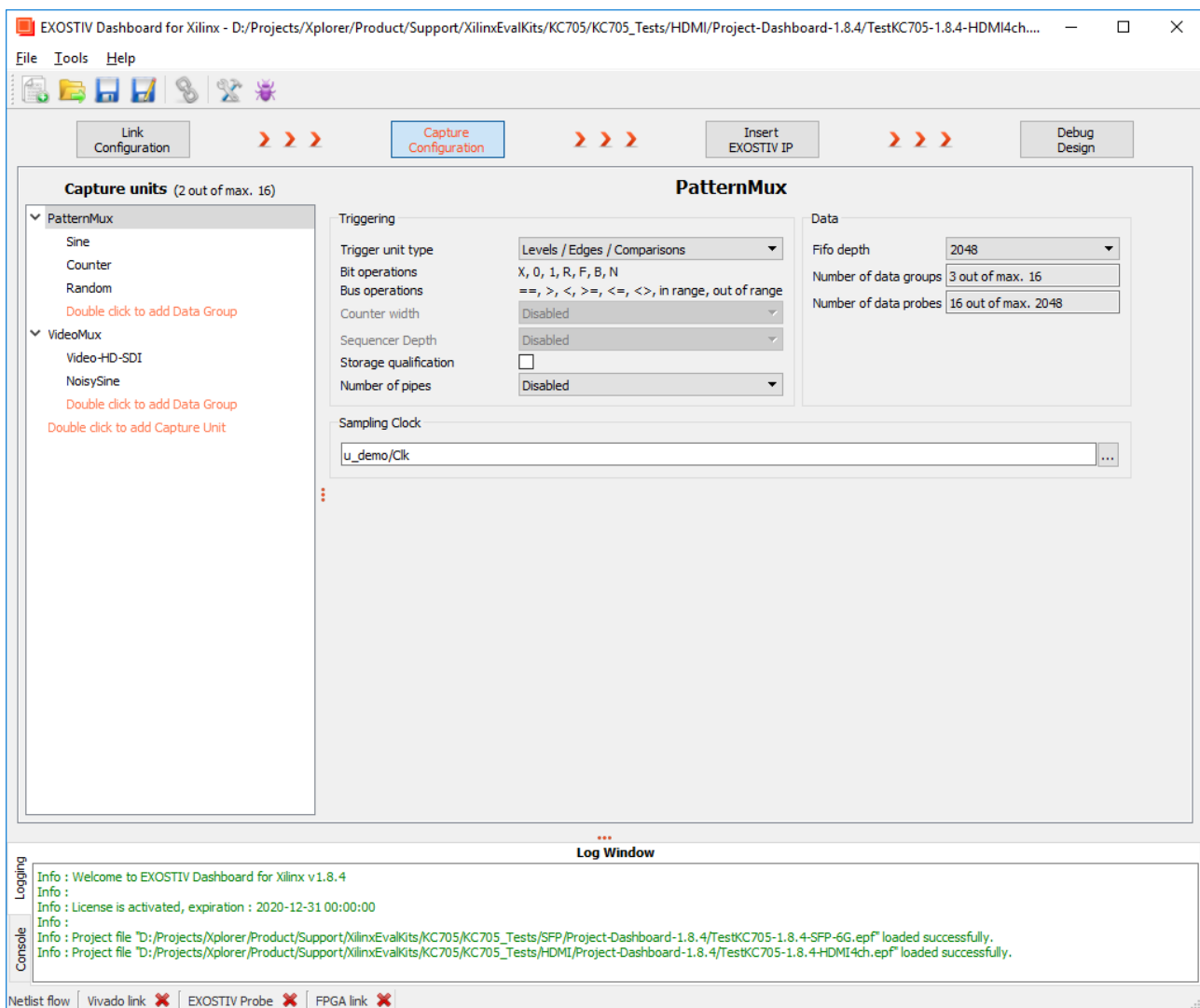
Console  
essfully.  
uccessfully.

Netlist flow | Vivado link ❌ | EXOSTIV Probe ❌ | FPGA link ❌

## Reviewing the .epf files settings for the capture configuration

Please open the .epf files and review them through the EXOSTIV Dashboard interface.  
Here are the main characteristics of the example:

- There are 5 data generators in the example design. There are connected to 2 capture units:
  - o 'Pattern', 'PatternMux' or 'System' Capture Unit (16 bits):
    - Digital sine wave: 'Sine' data group
    - A counter: 'Cnt' data group
    - A pseudo random number generator: 'Rnd' data group
  - o 'Video' or 'VideoMux' Capture Unit (46 bits):
    - Video (SDI) stream : 'HD-SDI' data group
    - Optionally, a Sine wave with noise : 'Noisy sine'.



The screenshot shows the EXOSTIV Dashboard for Xilinx interface. The main window is titled "EXOSTIV Dashboard for Xilinx - D:/Projects/Xplorer/Product/Support/XilinxEvalKits/KC705/KC705\_Tests/HDMI/Project-Dashboard-1.8.4/TestKC705-1.8.4-HDMI4ch...". The interface includes a menu bar (File, Tools, Help) and a toolbar with icons for file operations and a bug report. Below the toolbar are navigation buttons: "Link Configuration", "Capture Configuration" (highlighted), "Insert EXOSTIV IP", and "Debug Design".

The main configuration area is titled "PatternMux" and is divided into several sections:

- Capture units (2 out of max. 16):** A list on the left shows "PatternMux" and "VideoMux" units. Under "PatternMux", there are "Sine", "Counter", and "Random" data groups. Under "VideoMux", there are "Video+HD-SDI" and "NoisySine" data groups. Red text indicates "Double click to add Data Group" and "Double click to add Capture Unit".
- Triggering:**
  - Trigger unit type: Levels / Edges / Comparisons
  - Bit operations: X, 0, 1, R, F, B, N
  - Bus operations: ==, >, <, >=, <=, <>, in range, out of range
  - Counter width: Disabled
  - Sequencer Depth: Disabled
  - Storage qualification:
  - Number of pipes: Disabled
- Data:**
  - Fifo depth: 2048
  - Number of data groups: 3 out of max. 16
  - Number of data probes: 16 out of max. 2048
- Sampling Clock:** u\_demo/Clk

At the bottom of the interface is a "Log Window" with a "Logging" section and a "Console" section. The logging section shows:
 

```
Info : Welcome to EXOSTIV Dashboard for Xilinx v1.8.4
Info :
Info : License is activated, expiration : 2020-12-31 00:00:00
Info :
```

 The console section shows:
 

```
Info : Project file "D:/Projects/Xplorer/Product/Support/XilinxEvalKits/KC705/KC705_Tests/SFP/Project-Dashboard-1.8.4/TestKC705-1.8.4-SFP-6G.epf" loaded successfully.
Info : Project file "D:/Projects/Xplorer/Product/Support/XilinxEvalKits/KC705/KC705_Tests/HDMI/Project-Dashboard-1.8.4/TestKC705-1.8.4-HDMI4ch.epf" loaded successfully.
```

 At the very bottom, there are status indicators for "Netlist flow", "Vivado link", "EXOSTIV Probe", and "FPGA link", each with a red 'X' icon.

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