EXOSTIV Dashboard Hands-on - MICA board

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Revision History

Revision	Modifications
1.0.0	Initial revision
1.0.1	Minor updates
1.0.2	Update for EXOSTIV Dashboard v. 1.5.3Added section describing the RTL flow.
1.0.3	Update for EXOSTIV Dashboard v. 1.5.4
1.0.4	General review and update
1.0.5	Update for EXOSTIV Dashboard v. 1.9.1
1.0.6	Legal and brand names update.
1.0.7	Update with new versions of software



EXOSTIV Dashboard – Hands-on

Introduction

This session provides a documented practical example on how to use EXOSTIV Dashboard software for Xilinx FPGA.

In this session, we review the general flow used by EXOSTIV to instrument FPGA and extract debug data out of it.

Then we show how to use EXOSTIV Analyzer with a pre-configured demonstration board and configuration.

Finally, we describe how to use EXOSTIV Dashboard 'Core Inserter' to configure and insert a simple EXOSTIV IP core into a reference design.

EXOSTIV for Xilinx FPGA – Overview

Typically, the target FPGA design is instrumented with an 'EXOSTIV IP' core after synthesis or from the RTL source code. This IP is configured with the EXOSTIV Dashboard core inserter to reach FPGA internal nodes, sample them and send the sampled data to outside with gigabit transceivers.

Unlike JTAG-based solution, this approach does not require growing the FPGA memory resources with the size of the capture, as the recorded data is progressively extracted towards a memory located outside of the target FPGA. When the average required bandwidth does not exceed what the reserved transceivers are capable of, data can be extracted from the FPGA as a continuous flow or in bursts until the external memory is full.

Netlist flow



RTL flow

Figure 1: EXOSTIV for Xilinx FPGA – flows overview

2 alternate flows can be used with EXOSTIV: the 'RTL flow', and the 'netlist flow':

- The 'RTL flow' (or 'HDL flow') is used to insert the EXOSTIV IP in the RTL (VHDL or Verilog) source code. EXOSTIV Dashboard software is used to set up a generic IP provided as an output netlist and a top-level component (VHDL) or module (Verilog). This output IP has to be instantiated 'manually' in the source RTL code - after which the synthesis and implementation of the design are to be run.
- The 'netlist flow' is used to insert the EXOSTIV IP into a synthesized target design (= in the target design netlist). EXOSTIV Dashboard is used to configure the EXOSTIV IP and to insert / connect it in the target design netlist. This flow is more automatically managed from the EXOSTIV Dashboard and does not require any manual insertion. From a flow point of view, it has the advantage to work from a synthesized design – and hence – to save the time needed to synthesize the target FPGA every time a new EXOSTIV IP must be inserted. Once the target design



netlist is instrumented with EXOSTIV IP, it has to be implemented (place, route, bitstream generation). This flow is depicted at at

- Figure 1.

The general structure of EXOSTIV is depicted at **Figure 2**. With a large external 8GB memory, EXOSTIV provides up to 200,000 times more visibility than tradition embedded instrumentation solutions.

Figure 3 shows the general structure of the EXOSTIV IP core inserted into the FPGA.





The MICA board setup

Board Overview

The 'MICA' board is a compact target board that can be used to get started with EXOSTIV and demo the system. It is pre-configured with an example FPGA design.

The 'MICA' board is a target board mounted with an Artix-7 FPGA. Features:

- Artix-7 FPGA xc7a35tcsg325-2
- Micro-HDMI type connector, with 3 GTP lines for use with EXOSTIV Dashboard. The board power is supplied through this connector by the EXOSTIV probe.
- JTAG interface to reprogram the FPGA and the FPGA configuration EEPROM
- FPGA configuration EEPROM, pre-loaded with an example configuration for demo.



Connecting the board to the EXOSTIV probe

- 1. Place the HDMI to micro HDMI adapter on one end of the HDMI cable
- 2. Plug the HDMI end into the EXOSTIV probe HDMI connector and the micro-HDMI end into the MICA board





This setup can be used for demonstrating EXOSTIV: up to 3 transceivers are connected to the EXOSTIV probe through the HDMI connector and cables. The MICA board is powered through this cable too. Providing power through the HDMI cable requires using the proper option setting from EXOSTIV Dashboard (see Options menu).

Connecting the configuration cable to the MICA board

The demonstration kit includes a JTAG programming cable adapter for configuring the MICA board FPGA and its configuration EEPROM. This is only necessary when the FPGA configuration has to be changed.

It has to be connected to the PC with the provided micro USB cable. Please check the following article to know how to update the MICA board configuration: <u>https://www.exostivlabs.com/knowledgebase/how-do-i-update-the-mica-board-configuration/</u>







Quick Start – Run simple captures from the MICA board

This section of the tutorial shows how to use the MICA board setup with its standard configuration for capturing data with EXOSTIV Analyzer. This part loads a predefined project and does not use the EXOSTIV Core Inserter, which is described later in this document, from on page 19.

Demonstration kit contents and files

The demonstration kit includes:

- 1. 1x EXOSTIV probe with a power supply
- 2. 1x USB 3.0 cable for the EXOSTIV probe
- 3. 1x HDMI cable
- 4. 1x HDMI to mico-HDMI adapter
- 5. 1x MICA FPGA board
- 6. 1x programming kit for the MICA board

The following software and files are used with the demonstration kit:

Vivado v.2015.4 or	Please go to www.xilinx.com to download the software. The Vivado Webpack (free) is ok for using this
newer	demonstration kit. You'll need to register to download the software.
(from 2018.2	
recommended)	
FXOSTIV Deshboard v	Place download from this page, https://www.ovortiv/abs.com/cumpart/downloads/
EXUSTIV Dashboard V.	Please download from this page. <u>https://www.exostimabs.com/support/downloads/</u>
1.9.1 or newer	
	Please contact <u>support@exostivlabs.com</u> to receive the latest download link and a license key.
	Please check the 'UG501 - Getting started guide' for installation instructions.
EXOSTIV Dashboard	Please download from this page: https://www.exostivlabs.com/support/downloads/
reference project file	File archive - Domo MICA 2links 1.0 x zin
reference project file	
	Files:
	demo_mica702-3links-1.9.1.epf (or newer): EXOSTIV Dashboard project file.
	*.xml : EXOSTIV MYRIAD Waveform Viewer wave formatting files.
	Includes the MICA beard binaries : dome mice 702 2links 1.9.1 bin and dome mice 702 2links
	1.0.1 is the wire board bilanes. demo_mca/oz-sinks-1.5.1.5in and demo_mca/oz-sinks-
	1.9.1.Dit – Or newer.
	The MICA board is pre-configured. Use these files if the board configuration was changed and you want
	to revert back to the original configuration.
MICA board Artix-7	Please download from this page: https://www.exostivlabs.com/support/downloads/
FPGA reference design	File archive: DEMO MIC A7 02-export.zip

Overview of the reference design used for the demo instrumented with EXOSTIV IP.



Figure 4 : Overview of the reference design instrumented with EXOSTIV IP.

REMARKS:

- 1) The original design provided in the DEMO_MIC_A7_02-export.zip Vivado project does not include the EXOSTIV IP inserted.
- 2) The binary files provided as demo_mica702-3links.bit and demo_mica702-3links.bin include the EXOSTIV IP. The MICA board is provided pre-configured with these files.

Start EXOSTIV Dashboard and load the reference project file

All project files used with the EXOSTIV Dashboard contains the settings of one EXOSTIV IP.



- 2. On the Welcome Screen, click on 'Open Project'
- 3. Locate and load 'demo_mica702-3links-1.9.1.epf'



The Dashboard opens on the Core Inserter 'Link Configuration' window. Please note that this example is based on the 'netlist flow'.

Link			1					
figuration	<u>} </u>	Capture Configuration	2	<u>></u> >	Insert EXOSTIV IP	>>>	Debug Design	
		Connector						
Artix-7	-	Connector type	HDMI	•				
csg325	•							
-2	•							
xc7a35tcsg325-2	-							
		Downstream Link	-					
ank 216	-	Use I2C link	O Use transcei	ver link				
GTP		SCL package pin	M2	~				
H2		SDA package pin	M1	~				
F2		SCL I/O standard	LVCMOS18	•				
D2		SDA I/O standard	LVCMOS18	•				
B2		I/O voltages belo level shifter.	w 2.5V requires	an external				
ank 216 P0 D6 P1 B6 H2) 100 Range : 60 MHz (s) 5 (s) 15 QPLL coutput	▼ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓							
				•••				
e to EXOSTIV Dashboard	for Xilinx v1.8.2		Lo	g Window				
	TOT FOR IN VALUE							
	Artix-7 csg325 -2 xc7a35tcsg325-2 ank 216 GTP H2 F2 D2 B2 ck ank 216 P0 D6 P1 B6 H2 100 Range: 60 MHz s) 5 s) 15 QPLL cutput	Artix-7 csg325 -2 -2 xc7a35tcsg325-2 ank 216 (TP H2 F2 D2 B2 Ck ank 216 P0 B6 P1 B6 P1 B6 P1 B6 P1 B6 P1 B6 P1 S S S S S S S S S S Ange: 60 MHz to 660 MHz S S S S S S S S S S S S S	Artix-7 csg325 · -2 xc7a35tcsg325-2 Downstream Link ① Use I2C link SCL package pin SDA p	Artix-7 csg325 -2 xc7a3Stcsg325-2 ank 216 GTP H2 SCL package pin M2 SCL package pin M1 SCL I/O standard LVCMOS18 SDA JO standard LVCMOS18 SDA I/O standard LVCMOS18 I/O voltages below 2.5V requires a dec ank 216 P0 D6 P1 B6 P1 B6 P1 B6 P1 B6 P1 B6 P1 B6 P1 S5 S5 S5 S5 S5 S5 S5 S5 S5 S5	Artix-7 csg325 -2 xc7a3Stcsg325-2 ank 216 GTP H2 D2 B2 Connector Connector type HDMI Connector type HDM	Artix-7 csg325 -2 xx7a35tsg325-2 -2 xx7a35tsg325-2 -2 xx7a35tsg325-2 -2 xx7a35tsg325-2 -2 -2 xx7a35tsg325-2 -2 -2 -2 -2 -2<	Artix-7 cg325 -2 -2 xc7a351csg325-2 Downstream Link Image: Connector Ownstream Link Image: Connector Image: Connector Downstream Link Image: Connector Image: Connector Downstream Link Image: Connector Image: Connector Downstream Link Image: Connector Image: Connector Image: Connector Downstream Link Image: Connector Image: C	Artix-7 2 2: xc7a35tcsg325-2 Downstream Link Image: Sol Mate to 660 Mate Sol P1 B6 P1 B6 P1 B6 P1 B6 P2 D0 P3 Sol P4 P2 D2 D3 Sol P1 B6 P2 P3 B6 P4 P4 P5 P6 P1 B6 P1 B6 P1 B6 P1 B6 P1 B6 P2 P3 B6 P4 P4 P5 P6 P1 B6 P1 B6 P1 B6 P2 P3 B7 P4 P5 P6 P7 P8 P8 P9 P1 B6 P1 B6 P2 P3 P4 P4 P5 P6 P7 P8 P8 P8 P8 P8 P9 P8 P8 P8

EXOSTIV IP configuration review

The 3 buttons on the top of the window show the flow for configuring EXOSTIV IP, run insertion and then use the EXOSTIV Dashboard analyzer.

The steps required to configure and insert an IP are detailed from section 'Creating a 'netlist flow' project with EXOSTIV' at page 19 below.



Clicking on the 'Link Configuration' and 'Capture Configuration' buttons switch the display and allow to check the EXOSTIV IP configuration as defined in the demonstration project and loaded into the MICA demonstration board.

The overall settings match the description of Figure 4.



EXOSTIV Dachboard for Xilinx - Dr/Projects/X	nlorer/Hands-On/Demo-MIC/	-3links 1.8 v/demo. mica702-3lin	nks-182 enf				×
File Tools Help	piorei/riands-on/Demo-Mic/	-sinks_no.x/demo_mcaroz-sin	iks-1.0.2.epi				~
Link >>>	Capture Configuration	>>>	Insert EXOSTIV IP	>>>		ebug esign	
Capture units (3 out of max. 16)			Pattern				
✓ Pattern	Triggering			Data			
Cnt	Trigger unit type	Levels / Edges / Comparisons	-	Fifo depth	1024	•	
Sine	Bit operations	X, 0, 1, R, F, B, N		Number of data groups	3 out of max 16		
Noise	Bus operations	==, >, <, >=, <=, <>, in rang	e, out of range	Number of data groups	16 out of max. 2049		
Double click to add Data Group	Counter width	Disabled	~	Number of data probes	16 out of max. 2046		
✓ Video	Sequencer Depth	Disabled	Ψ.				
SDI	Storage qualification						
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Video-Extended	Sampling Clock						
Vid-Extended							
Double click to add Data Group						•••	
Double click to add Capture Unit							
	•						
L	1						
0		Log Window					
Info : Welcome to EXOSTIV Dashboard for Xilinx v	/1.8.2						
Info: Info: License is activated, expiration : 2020-12-3	1 00:00:00						
Info:	Domo MICA Slinke 1.9 v/domo m	ica 700, Slipka, 1, 9, 0, and loaded ave	constillu				
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ō							
Vetlist flow 🛛 Vivado link 💥 🗍 EXOSTIV Probe 💥 🏾	FPGA link 💥						



Switch to the EXOSTIV Dashboard Analyzer

The EXOSTIV Dashboard 'Analyzer' is used with the EXOSTIV Probe to sample and capture the internal nodes connected to the EXOSTIV IP.

Once you have loaded the target FPGA with the instrumented configuration, access the Analyzer by clicking on the 'bug icon' lets you access the EXOSTIV Analyzer.



Alternatively, the Analyzer can be accessed by clicking on 'Debug Design' in the top tool flow in the Core Inserter.



Connect the Probe

- 1. Connect the MICA board to the EXOSTIV probe
- 2. Power on the EXOSTIV Probe
- 3. Click on the 'connect' button in EXOSTIV Dashboard toolbar:
- 4. Click on 'Connect'

EXOSTIV Probe Connection	×
Probe found. Press 'Connect' to connect to the probe. Press 'Close' to continue without probe.	
searching for devices	Connect Close

Once connected to the probe, EXOSTIV automatically attempts to connect the probe to the IP that is in the target FPGA.

Info : Starting a link quality test for link S4 Info : Link quality test succeeded. Info : Info : Connected to EXOSTIV IP	
Netlist flow 🛛 Vivado link 💥 🗍 EXOSTIV Probe 🛩 🗍	FPGA link 🖌
EXOSTIV Dashboard is connected to the EXOSTIV Probe through USB	EXOSTIV Dashboard has found a valid EXOSTIV IP in the target design and there is A valid communication with it

Remarks:

- For the 'FPGA link' to be established, the EXOSTIV Probe must be able to:
- 1. properly communicate with an IP inserted in the target FPGA and:



- 2. check that the EXOSTIV IP inserted in the FPGA matches with the IP settings (CU, data groups, ...) as defined in the project file. For instance, if a project file is used, that does not match the EXOSTIV IP inserted in the FPGA, the communication will not be established and the EXOSTIV Dashboard Analyzer will not be usable. To check if the EXOSTIV IP inserted in the target FPGA matches with the project settings, a unique identifier (UUID) is programmed in the generated IP and read back with the EXOSTIV Probe. This UUID is also saved in the project file when a new EXOSTIV IP is generated.
- 3. The MICA board is powered through the HDMI link. The power line of the HDMI link is enabled through the EXOSTIV Dashboard menu: Tools > Menu

Options	×
Vivado	
Vivado Link Timeout	1 minute 🔹 💌
Capture Units Definition	
Confirm removing capture unit Confirm removing data group	N
EXOSTIV IP Insertion	
Auto save project on IP insertion	
On Application Close	
Confirm close	
Save project file Save wave configuration files	
HDMI Cable Setup	
Enable HDMI output power	
Miscellaneous Settings	
Digit grouping	, 👻
Restore Defaults Cancel	OK

To power on the MICA board, the project file **must** be loaded into the EXOSTIV Dashboard before attempting to connect to the EXOSTIV Probe. When the EXOSTIV Dashboard connects to the EXOSTIV Probe through USB, it first checks in the project settings if the HDMI cable should be used – and if the output power option is selected. If it is the case, the power is enabled before the probe attempts to communicate with the EXOSTIV IP loaded in the target FPGA.



Run a simple capture

- 1. Select 'Pattern' capture unit tab
- 2. Select 'Sine' Data Group
- 3. Select 'Stream to probe' Transfer mode
- 4. Specify 1 as number of captures
- 5. Specify the following number of samples per capture: 1999872
- 6. Set trigger position to 1022
- 7. Click on 'Run immediately'.

Pattern Video Vid	eo-Extended 1.	
	Data Group Selection	
	2.	
₽		
	Capture Cont	rol
Data		
Transfer mode	Stream to Probe	
Transfer mode Number of captures	Stream to Probe 1 to 238	3-6
Transfer mode Number of captures Samples per capture	Stream to Probe 1 1 to 238 1024 32 to 1,0	3. – 6 .)24
Transfer mode Number of captures Samples per capture Samples per capture	Stream to Probe 1 1 to 238 1024 32 to 1,0 1999872 1,024 to	3 6 .)24 477,218,560
Transfer mode Number of captures Samples per capture Samples per capture Trigger	Stream to Probe 1 1 to 238 1024 32 to 1,0 1999872 1,024 to	3. – 6 .)24 477,218,560
Transfer mode Number of captures Samples per capture Samples per capture Trigger Trigger position	Stream to Probe 1 1 to 238 1024 32 to 1,0 1999872 1,024 to 1022 2 to 1,99	3 6 . 124 477,218,560 99,870
Transfer mode Number of captures Samples per capture Samples per capture Trigger Trigger position Status	Stream to Probe 1 1 to 238 1024 32 to 1,0 1999872 1,024 to 1022 2 to 1,95	3. – 6.)24 477,218,560)9,870

The data is captured, uploaded to the PC and encoded as waves. They appear in the waveform viewer.

EXOSTIV Dashboard - C:/Projects/Xplorer/Hands-On/Demo-MICA-3links/demo_mica702-	inks.epf	- 6 ×
The Tools Help		
Pattern Video Video-Extended		
Data Group Scieccion	AND Equation	Output Equation
Sine •	Signal Name Operation	
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2 2 S Capture Control		
Data		
Number of captures		
Samples per capture 1024 22 to 1,024		
Samples per capture 23552 1,024 to 477,218,560	Use other capture units	
Trigger	🕂 💥 OR Equation	
Trigger position 8714 2 to 23,550	Signal Name Operation	
Status		
Status .		
Capture		
· ·		
» :		
Auto Export Captures	Use other capture units /	
	Wave Viewer	
	Any transition *	
a demo[0] u core/sine Data[15 EC22	-8300 -8400 -8500 -3800 -2700 -1800 -500 Q 900 1800 2700 3800 4800 5400	6300 7200 8100 9000 9900 10800 11700 12800 13506 14400
-g_demoloj.d_corersine_Data[10]E022		
900 1800	2700 3600 4500 5400 6300 7200 8100 9000 9000 10800 11700 12600 13500 1	1400 15300 16200 17100 18000 18900 19800 20700 21600 22500 2340
c b c b c	11775	2
Info : Starting a link quality test for link S4	Log Window	^
Info : Link quality test succeeded. Info :		
Into : Connected to EXOSTIV IP		v
Netlist flow 🛛 Vivado link 💢 🛛 EXOSTIV Probe 🛩 🖉 FPGA link 🛩		



8. Right-click on the sine_data bus in the waveform window and change radix to 'Analog' to display the digital sine wave as analog signal. Then do it again and select Color > Wave to change the wave color. This is a simple example of how the wave can be formatted.



As a result the Sine Wave is displayed as analog format, and can be expanded bit by bit as well...





Run a burst capture with trigger

- 1. Select 'Video' tab
- Select 'SDI' data group
 Set up a capture with e.g. 100 captures of 3584 samples
 Position trigger at sample 2345

Pattern	Video	Video-	Extended]		
			Data Gro	up Selec	tion	
₽₽	I					•
≥ ≥ Data	8			Captur	e Control	^
Transfer	mode		Stream to	Probe		•
Number	of captures	S	100		1 to 133,152	
Samples	per captur	e	2048	~	32 to 2,048	
Samples	per captur	e	3584		2,048 to 4,771,840	
Trigger						
Trigger p	osition		2345		2 to 3,582	
Status						
Status			-			
Capture						~

5. Go to the 'trigger controls' select the following pre-saved trigger equation:



		Signal Name		Operation
1		g_demo[0].u_core/sdi_Valid	== *	R b
	Use o	ther capture units 🖉 📉		
4			OR Equation	
		Signal Name		Operation
1	\checkmark	g_demo[0].u_core/sdi_SOF	== 🔻	R b
		g demo[0].u core/sdi HBlank	==	R b

6. Run the capture with trigger by clicking on the '>|' button:

ve Viewer																														-	٥
												Wave	e View	er																	
N 🐼 📈 🛞 🔍	\ominus \ominus	4	4		C					ny tra	nsition	-																			
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			1791	99																											
> <	> <																														

- 7. To change the wave formatting, click on the 'load wave format' button :
- 8. Locate an select file 'sdi.xml', open, then zoom...

0



Load Configuration File					×
\leftarrow \rightarrow \checkmark \Uparrow \checkmark \checkmark \land Projects \Rightarrow Xplorer \Rightarrow hardware	> fpga > DEMO_MIC_A7_02 > Demo-MICA	-3links > 💊	 Search Dem 	io-MICA-3links	Q
Organize 🔻 New folder				· · ·	?
.svn	^ Name	Date modified	Туре	Size	
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🔊 fpga	cnt.xml	8/4/2016 5:19 PM	XML Document	2 KB	
o_ac701_hfh_eeprom	noise.xml	8/4/2016 5:19 PM	XML Document	5 KB	
o ac701_ibert	🗋 rnd.xml	8/4/2016 5:19 PM	XML Document	2 KB	
o common	sdi.xml	8/18/2016 4:28 PM	XML Document	5 KB	
DEMO 01	sdi-ext.xml	8/17/2016 1:52 PM	XML Document	9 KB	
DEMO_01_local160203					
DEMO_03					
DEMO_MIC_A7_01					
DEMO_MIC_A7_02					
Demo-MICA-3links					
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] u_core/sdi_VBlank 0			
] u_core/sdi_Valid 1 [0] [0] [0] [0] [0] [0] [0] [0] [0] [0]	45 <u>(46)(47)</u>	(40)(41)(42)	
n a sea dar-dadada dar-dadadada dar-dadadada dar-dadadada dar-dadadada dar-dadadada dar-dadadada			
o[u_coreisa]_k[a:.0] zaa			
	ลลล		
0] u_core/sdi_G[90] 000			
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Creating a 'netlist flow' project with EXOSTIV Dashboard

In this section, we'll describe how to create a 'netlist flow' project from zero using EXOSTIV Dashboard. It shows how to configure an IP and insert it into the target design with EXOSITV Dashboard Core Inserter.

In this section, we'll use the MICA board reference design, Xilinx Vivado and the EXOSTIV Dashboard.

Start Vivado and create a new netlist flow project

Xilinx Vivado version 2015.4 or newer must be used. The free Webpack version is sufficient for this demonstration, as the Artix-7 FPGA device mounted on the MICA board is supported with this version.

1. Load the demonstration project 'DEMO03'

e F <u>l</u> ow <u>T</u> ools <u>W</u> indow <u>H</u> elp	
VIVADO. Productivity. Multiplied.	
Quick Start	
Create New Project Open Project Open Example Project	
Tasks	





2. In Vivado, open 'Synthesized Design'

A demo_03 - [P:/Xplorer/hardware/fpga/DEMO_MIC_A7_02	- export/impl/demo_03/demo_03.xpr] - Viv	vado 2016.2											-	٥	×
File Edit Flow Tools Window Layout View Help											Q- S	earch con	nmands		
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Flow Navigator ? «	Project Manager - demo_03													-	? X
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Project Manager	옥 🛣 🚔 🖬 🔂		Project Se	ttings											^
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😚 Add Sources			Project local	ion: P	:/Xplorer	/hardware	e/fpga/D	EMO_MIC	_A7_02 - expor	t/impl/dem	03				
V Language Templates	Constraints (3)		Product fam	ly: A	rtix-7										
IP Catalog	Imulation Sources (5)		Project part	×	c7a35tcs	q <u>325-2</u>									
			Top module	name: d	emo 03	N									
 IP Integrator 			: Target langu	iage: V	HDL										
🕂 Create Block Design	Hierarchy IP Sources Libraries Compil	le Order	Simulator lar	guage: N	lixed										
Propen Block Design	Properties	2	Synthesis						Im	olementa	tion				
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Run Simulation			Part:	xc7a35tcs	g325-2				Par	t:		xc7a35to	so325-2		
	Select an object to see	e properties	Strategy:	Vivado Syr	- nthesis D	efaults			Str	ateriv:		Vivado Im	plementat	ion Defa	ault
A RTL Analysis									Inc	remental co	mpile:	None			
K Elaboration Settings			<												>
Open Elaborated Design	Design Runs												? _	<u>п</u> .е	×
4 Synthesis	Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Failed Routes	LUT	FF	BRAM	URAM	DSP	Star
🍪 Synthesis Settings	Synth_1 (active)	constrs_1	synth_design Complete	4						724	959	(0 (0
🗞 Run Synthesis	impl_1	constrs_1	write_bitstream Complete!	0.829	0.000	0.056	0.000	0.000		0 728	1079	21	1 (3	0
Open Synthesized Design	Out-of-Context Module Runs Synth 1	blk mem w256 r8	synth design Complete!								0	4	4 1	0	0
	<pre>/d √ ck_gen_synth_1</pre>	dk_gen	synth_design Complete!							c	0			0	0
4 Implementation	ck_video_synth_1	clk_video	synth_design Complete!							C	0	(0	3	0
Mig Implementation Settings	✓ rom_sine_synth_1	rom_sine	synth_design Complete!							0	0	0))	0
Run Implementation	✓ rom sine 51b T4111 synth	1 rom sine 51b T411	1 synth design Complete!							24	53	1	1	0	0
Open Implemented Design	✓ rom_sine_67b_T2039_synth_:	1 rom_sine_67b_T203	9 synth_design Complete!							C	67	4	4 (a i	0
4 Program and Debug	E														>
Bitstream Settings V	🔚 Td Console 🖉 Messages 🛛 🔍 Log	g 🗋 Reports 🗊 🖡	esign Runs												

After some time, the synthesized reference design is loaded into Vivado.



3. Start EXOSTIV Dashboard



4. In the welcome screen, click on 'Create New Project'

EXOSTIV Dashboard for Xilinx				_		×
<u>File Tools H</u> elp						
		/				
EXOSTIV [™]	Reach. Store. Analyze.			EXOS FPGA Debug R	LABS eloaded	
1	-					
	<u>Create New Project</u> A wizard will help you create a new project.		eer Guide / Getting Started			
	Open Project Open an existing project.	?	<u>Knowledge Base</u> Online knowledge base.			
	Open Recent Project Open an recently used project.	P	<u>License</u> Manage licenses,			
		 Log Window				
Info : Welcome to EXOSTIV Dashboard for Xilinx v1.	8.2					
Info : License is activated, expiration : 2020-12-31	00:00:00					
No flow defined 🛛 Vivado link 💥 🗍 EXOSTIV Probe 💥	EPGA link 🞽					

The 'Create New Project' window appears, prompting to select the desired flow (Netlist flow or RTL flow)

🔲 New Proj	ect	?	×
Create N	New Project		
Type	Netlist IP insertion		
	The EXOSTIV IP is configured and inserted in the target design netlist.		
	The target design must be loaded after synthesis in the FPGA vendor tool.		
	EXOSTIV Core Inserter is used to select the nodes to be connected to the EXOSTIV IP.		
	EXOSTIV IP will be generated, synthesized and connected to the target netlist.		
	Implementation (place & route) and bitstream generation can optionally be started from EXOSTIV Dashboard.		
Name	mynewproject		
Create in	C:/Projects	Browse	
	Cancel	Creat	2



- Select 'Netlist IP Insertion' from the type drop-down box.
- Specify new project name and pick a location.
- For permission issues reasons please do not create project in Program Files (x86) or Program Files directory.

The 'Link Configuration window' of the core inserter appears.

EXOSTIV (Dashboard for Xilinx - Help	C:/Users/frede/new_pro	ject.epf					-	×
		2 🕷							
c	Link Configuration	>>>	Capture Configuration	2	> >	Insert EXOSTIV IP	2 2 2	Debug Design	
FPGA Type			Connector						
Family	Artix-7 - Defense-gr	rade 🔻	Connector type	HDMI	•				
Package	cs325	•							
Speed grad	de -11	• •							
Porc	xq7850(C8525-11								
Upstream L	ink		Downstream Link						
Transceive	er bank 216	-	() Use I2C link	Use transceiv	ver link				
MGT type	GTP		SCL package pin	A9	~				
MGT_TxP0	H2		SDA package pin	A9	~				
MGT_TxP1	F2		SCL I/O standard	LVCMOS33	•				
MGT_TxP2	D2		SDA I/O standard	LVCMOS33	•				
MGT_TxP3	B2								
Beference	Clock								
Transceius	ubaek 216	-							
MGT_REEC									
MGT REFC	CLK P1 B6								
Frequency	(MHz) 100	2							
	Range : 60 f	MHz to 660 MHz							
Line rate (0	Gb/s) 3.2	•							
Link rate (O	Gb/s) 0								
PLL type us EXOSTIV d	sed QPLL								
2.001110									
				Log	Window				
odgine									
-									
Isole									
Co									
Netlist flow Viv	vado link 💥 🛛 EXOSTI	V Probe 💥 🛛 FPGA link	×						

Using the Core Inserter

Overview

To access the 'Core Inserter', click on the following icon in the main toolbar:

Inserting the EXOSTIV IP requires 3 successive steps:

- Step 1 : Link Configuration
- Step 2 : Capture Configuration
- Step 3 : Run Insertion

These 3 steps are accessible through the top flow overview in the EXOSTIV Dashboard window

	Link Configuration	>>>	Capture Configuration	>>>	Insert EXOSTIV IP	2.2.2	Debug Design
L .,							



Step 1: Link Configuration

This step defines the characteristics of the target FPGA and of the interface between EXOSTIV IP and EXOSTIV Probe. The information required to complete this step depends on the target FPGA and the target FPGA board. For this hands-on session, we'll use the MICA board from Exostiv Labs. Please refer to the MICA 702 board user's guide for a details (<u>https://www.exostivlabs.com/files/documents/Demo%20Kit%20User's%20Guide%20-%20MICA702.pdf</u>).

Please set up as follows: 1. FPGA Type

FPGA Type	
Family	Artix-7 🔻
Package	csg325 👻
Speed grade	-2 🔻
Part	xc7a35tcsg325-2 👻

2. Connector : HDMI, as we'll use the HDMI type of connection between the MICA board and EXOSTIV Probe

Connector	
Connector type	HDMI 🔻

3. Upstream link: this setting defines the location of the used gigabit transceivers on the FPGA package. In this case, we'll use the transceivers connected to the micro-HDMI on the MICA board. They are at sites H2, F2 and D2 of bank 216.

Upstream Link		
Transceiver bank	216 👻	
MGT type	GTP	
MGT_TxP0	H2	3
MGT_TxP1	F2	1
MGT_TxP2	D2	1
MGT_TxP3	B2]

4. Downstream link: this setting defines the location of the 2 pins connected to the micro-HDMI connector used for the downstream 'I2C-like' link used to configure EXOSTIV IP at run time. SCL and SDA are respectively at sites M2 and M1 of the Artix-7 FPGA package. The I/O standard is LVCMOS18.

Downstream Link						
● Use I2C link ○ Use transceiver link						
SCL package pin	M2	~				
SDA package pin	M1 .	~				
SCL I/O standard	LVCMOS18	•				
SDA I/O standard	LVCMOS18	•				
I/O voltages belov shifter.	v 2.5V require an external lev	e/				



5. **Reference Clock:** this defines the pin input of the reference clock used for the transceiver used for EXOSTIV, as well as its frequency (100 MHz). From the frequency, we can choose the link rate setting. We choose the maximum link rate available for this frequency / FPGA / EXOSTIV Probe model, that is 5 Gbps.

Reference Clock	
Transceiver bank	216 👻
MGT_REFCLK_P0	D6
MGT_REFCLK_P1	B6
Frequency (MHz)	100
	Range : 60 MHz to 660 MHz
Line rate (Gb/s)	5 💌
Link rate (Gb/s)	15
EXOSTIV clock output	

Here is an overview of the 'Link Configuration' for this example:

EXOSTIV Dashboard f	for Xilinx - D:/Projects/Xplorer/Han	ds-On/Demo-MICA	-3links_1.8.x/den	no_mica702-3li	nks-1.8.2.epf		-	×
Link Configuration	>>> 20 25 ∰	Capture Configuration	2.2	2	Insert EXOSTIV IP	>>>	Debug Design	
FPGA Type		Connector						^
Family Artix-7	•	Connector type	IDMI	•				
Package csg325	•							
Speed grade -2	•							
Part xc7a35tc	sg325-2 🔻							
Upstream Link		Downstream Link						
Transceiver bank 216	•	Use I2C link	Use transceive	er link				
MGT type GTP		SCL package pin	M2	~				
MGT_TxP0 H2		SDA package pin	M1	~				
MGT_TxP1 F2	\checkmark	SCL I/O standard	LVCMOS18	•				
MGT_TxP2 D2	\checkmark	SDA I/O standard	LVCMOS18	•				
MGT_TxP3 B2		I/O voltages belov level shifter.	v 2.5V requires an	external				
Reference Clock								
Transceiver bank	216 🔻							
MGT_REFCLK_P0	D6							
MGT_REFCLK_P1 E	36							
Frequency (MHz)	100 🥑							
Line rate (Gb/s)	5 💌							
Link rate (Gb/s)	15							
PLL type used Q EXOSTIV dock output	2PLL							
								~
2			Log	Window				
명 Info : Welcome to EXOS	TIV Dashboard for Xilinx v1.8.2							
Info : License is activate Info :	ed, expiration : 2020-12-31 00:00:00							
Info : Project file "D:/Pro	ojects/Xplorer/Hands-On/Demo-MICA-	-3links_1.8.x/demo_mi	a702-3links-1.8.2	epf" loaded suc	ccessfully.			
Netlist flow 🛛 Vivado link 💢	🛛 🛛 EXOSTIV Probe 🗶 🗍 FPGA link 🖇	ĸ						



✓ LINK CONFIGURATION: DONE !

To save the project:

Step 2 : Capture Configuration

This part of the flow defines the characteristics of the EXOSTIV IP core – namely:

- The capture units and their features:

- Trigger resources
- Enable / Disable storage qualification
- o FIFO depth
- The sampling clock for each capture unit
- o ...
- The data groups for each capture units and the signals from the target design that are part of each data group

EXOSTIV Dashboard - C:/Projects/mynewproject.epf			- 1	- ×
Link Configuration	>>>	Insert >>>	Debug Design	
Capture units (1 out of max. 16)	Capture U	Jnit 1		
Capture Unit 1		Data		
Data Group I Trigger unit type	Levels / Edges 🔻	Fifo depth 1024	•	
Double click to add Data Group Bit operations	X, 0, 1, R, F, B, N	Number of data groups 1 out of max. 16		
Double click to add Capture Unit Bus operations	==	Number of data probes 0 out of max. 2048		
Counter Width	Disabled			
Storage gualification				
Number of pipes	Disabled 🔻			
ampling Clock				
Select capture unit to see its main features				
	•••			
Tafe a License is activated evaluation - 2020-01-01-00-00-00	Log Window			
Into: License is acuvated, expiration : 2020-01-0100:000	l call i maati 71 j			^
Into : Project file "C:/Projects/Xplorer/hardware/fpga/DEMO_MIC_A7_02/test/Mica-3lin Info : Project file "C:/Projects/mynewproject.epf" loaded successfully.	ks-v1.5/demo_mica702-3links.epf" load	led successfully.		
				~
Netlist flow 🛛 Vivado link 💢 🛛 EXOSTIV Probe 💢 🛛 FPGA link 💢				



For 'Capture Unit 1', select the following:

- 1. Trigger unit type: Levels / Edges / Comparisons
- 2. Fifo Depth : 1024
- 3. Leave the other settings as they are.
- 4. Double-click on the Capture Unit name to change it. Change it to 'Pattern'.
- 5. Click on the data group name to define or see the connected nodes
- 6. Double-click on the Data Group name to change it. Change it to 'Sine'.

EXOSTIV Dashboard - C:/Projects/mynewproject.epf	-	
Link Capture Insert Configuration Configuration Configuration	Debug Design	
Capture units (1 out of max. 16) Data Group 1		
Capture Unit 1 Edit Probes		
Data Group 1	Data	Trigger
Double click to add Capture Unit	Data	nigger
Select data group to define / see connected nodes		
C		>
Log Window		
Info : License is activated, expiration : 2020-01-01 00:00:00		^
ا ۱۳۵۱ : Info : Project file "C:/Projects/Xplorer/hardware/fpga/DEMO_MIC_A7_02/test/Mica-3links-v1.5/demo_mica702-3links.epf" loaded successfully.		
Info : Project file "C:/Projects/mynewproject.epf" loaded successfully.		
Netlist flow 🛛 Vivado link 💥 🗍 EXOSTIV Probe 💥 🗍 FPGA link 💥		

Capture units (1 out of max. 16)





🔲 EXOSTIV Dashboard - C:/Users/frederic/new_project.epf — 🗆 🗙									
jile <u>T</u> ools <u>H</u> elp									
🗟 🔚 🔚 😓 😤 💥									
Link Configuration	Capture Configuration	>>>	Insert EXOSTIV IP	<u>> > ></u>	Debug Design				
Capture units (1 out of max. 16)			Data Group 1						
✓ Pattern	Edit Probes								
Sine	Signal Names				Data	Trigger			
Double click to add Data Group									
Double click to add Capture Unit									
	:								
	<					3	>		
		Log Window							
Info : Info : Probe disconnected		-					^		
Info : Project file "C:/Projects/Xplorer/Hands-On/Demo-MICA	A-3links/demo_mica702-3links.epf" written success	fully.							
Into : Project file "C:/Users/frederic/new_project.epf" writte	n successfully.						~		
Netlist flow 🛛 Vivado link 💥 🗍 EXOSTIV Probe 💥 🗍 FPGA	link X								

7. We now have to connect EXOSTIV Dashboard to Vivado, in order to select the nodes to be observed. Switch back to Vivado and click on 'EXOSTIV Dashboard' shortcut in the main toolbar.

🍌 demo_03 - [P:/Xplorer/hardware/fpga/DEMO_MIC_A7_02	- export/impl/demo_03/demo_03.xpr] - Vivado 2016.2	
<u>File Edit Flow Tools Window Layout View Help</u>		
😂 🖿 i in 🕫 🐂 🐂 🗙 🛷 i 🔈 🎦 🍏	🗘 🥝 🆚 💥 📡 🍕 😬 Default Layout 🔹	- X 🚸 🔭 🔳 🔍
Flow Navigator ? «	Synthesized Design - synth_1 xc7a35tcsg325-2 (active)	
	N-12-1	

8. In the 'EXOSTIV Dashboard Launcher' window, select the running instance of the EXOSTIV Dashboard and click on 'Link to Vivado'. This establishes a link between Vivado and EXOSTIV Dashboard.

EXOSTIV Dashboard L	auncher				_		Х
Link to Vivado Bring T	To Front	New Dashboard		Location Network		Quer	y
Host Name 8piclt15	IP Address 192.168.0.8	Local yes	Pid 7968	Project File P:/Xplorer/hardware/fpga/DEMO_MIC	_A7_02/tr	est/demo	mi



Info : Replied to Vivado query packet. Info : Received link to Vivado request. Info : Successfully connected to Vivado. Info : Acknowledged link to Vivado request.
Netlist flow 🛛 Vivado link 🛩 🗍 EXOSTIV Probe 💥 🗍 FPGA link 💥

9. In EXOSTIV Dashboard, select the 'Sine' data group and click on 'Edit Probes'

[
EXOSTIV Dashboard - P:/Xplorer/hardware/fp	ga/DEMO_MIC_A7_02/test/demo_mica702-3links.epf	-		×
<u>F</u> ile <u>T</u> ools <u>H</u> elp				
🗟 📴 🖬 📓 🗞 💥 🕷				
Link Configuration	Configuration	Debug Design		
Capture units (1 out of max. 16)	Sine			
✓ Pattern	Edit Probes			
Sine	Signal Names	Data	Trigg	ger
Double click to add Capture Unit				

10. From the 'Connect Probes' window, browse the design and select the signal 'u_demo/sine_Data[15:0]

Connect Probes			
Design Hierachy			
✓ demo_03_N			^
g_demo[0].u_core			
> u_color			
> u_noisy			
u_noisy_2			
u_period			
> u_ram			
u_rnd			
> u_rom1			
> u_rom2			
u_sample			
u_shuffle_sync			
> u_sine			
u wr sync		eee	Ť
Filter 🔍 sine_d			
Found Signals		Data Signals	
Found Signals sine_Data[3]_i_1_n_0	^	Data Signals g_demo[0].u_core/sine_Data[150]	
Found Signals sine_Data[3]_i_1_n_0 sine_Data[4]_i_1_n_0	^	Data Signals g_demo[0].u_core/sine_Data[150]	
Found Signals sine_Data[3]_i_1_n_0 sine_Data[4]_i_1_n_0 sine_Data[5]_i_1_n_0	^	Data Signals g_demo[0].u_core/sine_Data[150]	
Found Signals sine_Data[3]_i_1_n_0 sine_Data[4]_i_1_n_0 sine_Data[5]_i_1_n_0 sine_Data[6]_i_1_n_0	^	Data Signals g_demo[0].u_core/sine_Data[150]	
Found Signals sine_Data[3]_i_1_n_0 sine_Data[4]_i_1_n_0 sine_Data[5]_i_1_n_0 sine_Data[6]_i_1_n_0 sine_Data[7]_i_1_n_0	^	Data Signals g_demo[0].u_core/sine_Data[150]	
Found Signals sine_Data[3]_i_1_n_0 sine_Data[4]_i_1_n_0 sine_Data[5]_i_1_n_0 sine_Data[6]_i_1_n_0 sine_Data[7]_i_1_n_0 sine_Data[8]_i_1_n_0	^	Data Signals g_demo[0].u_core/sine_Data[150]	
Found Signals sine_Data[3]_i_1_n_0 sine_Data[4]_i_1_n_0 sine_Data[5]_i_1_n_0 sine_Data[6]_i_1_n_0 sine_Data[7]_i_1_n_0 sine_Data[8]_i_1_n_0 sine_Data[9]_i_1_n_0	^	Data Signals g_demo[0].u_core/sine_Data[150] Click on arrow to place signal in	
Found Signals sine_Data[3]_i_1_n_0 sine_Data[4]_i_1_n_0 sine_Data[5]_i_1_n_0 sine_Data[6]_i_1_n_0 sine_Data[7]_i_1_n_0 sine_Data[8]_i_1_n_0 sine_Data[9]_i_1_n_0 sine_Data[10]_i_1_n_0	^	Data Signals g_demo[0].u_core/sine_Data[150] Click on arrow to place signal in the 'Data Signals list'	
Found Signals sine_Data[3]_i_1_n_0 sine_Data[4]_i_1_n_0 sine_Data[5]_i_1_n_0 sine_Data[6]_i_1_n_0 sine_Data[7]_i_1_n_0 sine_Data[8]_i_1_n_0 sine_Data[9]_i_1_n_0 sine_Data[10]_i_1_n_0 sine_Data[11]_i_1_n_0	^	Data Signals g_demo[0].u_core/sine_Data[150] Click on arrow to place signal in the 'Data Signals list'	
Found Signals sine_Data[3]_i_1_n_0 sine_Data[4]_i_1_n_0 sine_Data[5]_i_1_n_0 sine_Data[6]_i_1_n_0 sine_Data[7]_i_1_n_0 sine_Data[8]_i_1_n_0 sine_Data[9]_i_1_n_0 sine_Data[10]_i_1_n_0 sine_Data[11]_i_1_n_0 sine_Data[12]_i_1_n_0	Select	Data Signals g_demo[0].u_core/sine_Data[150] Click on arrow to place signal in the 'Data Signals list'	
Found Signals sine_Data[3]_i_1_n_0 sine_Data[4]_i_1_n_0 sine_Data[5]_i_1_n_0 sine_Data[6]_i_1_n_0 sine_Data[7]_i_1_n_0 sine_Data[9]_i_1_n_0 sine_Data[9]_i_1_n_0 sine_Data[10]_i_1_n_0 sine_Data[11]_i_1_n_0 sine_Data[12]_i_1_n_0 sine_Data[13]_i_1_n_0 sine_Data[13]_i_1_n_0	Select	Data Signals g_demo[0].u_core/sine_Data[150] Click on arrow to place signal in the 'Data Signals list'	
Found Signals sine_Data[3]_i_1_n_0 sine_Data[4]_i_1_n_0 sine_Data[5]_i_1_n_0 sine_Data[6]_i_1_n_0 sine_Data[7]_i_1_n_0 sine_Data[9]_i_1_n_0 sine_Data[10]_i_1_n_0 sine_Data[11]_i_1_n_0 sine_Data[12]_i_1_n_0 sine_Data[13]_i_1_n_0 sine_Data[14]_i_1_n_0 sine_Data[14]_i_1_n_0	Select	Data Signals g_demo[0].u_core/sine_Data[150] Click on arrow to place signal in the 'Data Signals list'	
Found Signals sine_Data[3]_i_1_n_0 sine_Data[4]_i_1_n_0 sine_Data[5]_i_1_n_0 sine_Data[6]_i_1_n_0 sine_Data[9]_i_1_n_0 sine_Data[9]_i_1_n_0 sine_Data[10]_i_1_n_0 sine_Data[11]_i_1_n_0 sine_Data[12]_i_1_n_0 sine_Data[13]_i_1_n_0 sine_Data[14]_i_1_n_0 sine_Data[15]_i_2_n_0	Select	Data Signals g_demo[0].u_core/sine_Data[150] Click on arrow to place signal in the 'Data Signals list'	
Found Signals sine_Data[3]_i_1_n_0 sine_Data[4]_i_1_n_0 sine_Data[5]_i_1_n_0 sine_Data[6]_i_1_n_0 sine_Data[7]_i_1_n_0 sine_Data[9]_i_1_n_0 sine_Data[10]_i_1_n_0 sine_Data[11]_i_1_n_0 sine_Data[12]_i_1_n_0 sine_Data[13]_i_1_n_0 sine_Data[14]_i_1_n_0 sine_Data[15.0]	Select	Data Signals g_demo[0].u_core/sine_Data[150] Click on arrow to place signal in the 'Data Signals list'	
Found Signals sine_Data[3]_i_1_n_0 sine_Data[4]_i_1_n_0 sine_Data[5]_i_1_n_0 sine_Data[6]_i_1_n_0 sine_Data[7]_i_1_n_0 sine_Data[9]_i_1_n_0 sine_Data[10]_i_1_n_0 sine_Data[11]_i_1_n_0 sine_Data[12]_i_1_n_0 sine_Data[13]_i_1_n_0 sine_Data[14]_i_1_n_0 > sine_Data[150]	Select	Data Signals g_demo[0].u_core/sine_Data[150] Click on arrow to place signal in the 'Data Signals list' Cancel Done	

11. If necessary, change the signal filter by clicking on the magnifier icon:



Connect Probes					
Design Hierachy		/			
✓ demo_03_N					^
g_demo[0].u_core					
> u_color					
> u_noisy					
u_noisy_2					
u_period					
> u_ram					
u_rnd					
> u_rom1					
> u_rom2					
u_sample					
u_shuffle_sync					
> u_sine					
wr svnc					¥
Filter sine d					
Found 🖌 All signals		1	Data Signals		
sit MARK_DEBUG signals	^	[g_demo[0].u_core/sine_Data[150]		
sii 🗸 Plain text					
si Plain text with wildcards					
si De la contra contra contra		8			
si Regular expression		-			
si Case sensitive		>>			
sine Data1101 i 1 n 0	1				
sine Data[11] i 1 n 0		**			
sine Data[12] i 1 n 0		<			
sine Data[13] i 1 n 0		-			
sine_Data[14]_i_1_n_0					
> sine_Data[150]					
sine_Data[15]_i_2_n_0	~				
Number of probes : 16				Cancel	Done

12. Select 'Pattern' capture unit and click on the '...' button to define the capture unit's sampling clock:

EXOSTIV Dashboard - C:/Projects/mynewpro	oject.epf				- 0	×
<u>F</u> ile <u>T</u> ools <u>H</u> elp						
🗟 🖻 🗖 🖉 🗞 💥						
Link Configuration	Capture Configuration	>>>	Insert EXOSTIV IP	2 2 2	Debug Design	
Capture units (1out of max. 16)		Р	attern			
Y Pattern	Triggering			Data		
Sine	Trigger unit type	Levels / Edges / Comparisons	▼	Fifo depth 1.24	-	
Double click to add Data Group	Bit operations	X, 0, 1, R, F, B, N		Number of data groups 1 out	of max. 16	
boable circk to add capture onit	Counter width	==, >, <, >=, <=, <>, in range, Disabled	, out of range	Number of data probes 0 out	of nax. 2048	
	Sequencer Depth	Disabled	~			
	Storage qualification					
	Number of pipes	Disabled	•			
	Sampling Clock				×	
		Log Window				
Info : Replied to Vivado query packet. Info : Received link to Vivado request.						^
Info : Successfully connected to Vivado.						
and a Acciowicuged link to vivauo request.						~
Netlist flow 🛛 Vivado link 🖌 🗍 EXOSTIV Probe 💥 🏾	FPGA link 💢					.:



13. Select 'demo_03_N/Clk', bring it to the 'Clock signal' box with the '>' and click on 'Done'.

Connect Probes	
Design Hierachy demo_03_N > g_demo[0].u_core > u_clk u_reset u_shuffle_sync u_time u_vidrst > u_vid_mmcm	

Filter	
Found Signals	Clock Signal
Clk SysClk vid_Clk	
	Cancel Done

14. Set up 2 additional capture units, with the parameters of the table below (or load the reference project file 'demo_mica702-3links.epf' if you want to skip this step)

	Name	Trigger unit type	Storage qualification	Number of pipes	Fifo depth	Number of data groups	Number of data probes	Sampling Clock
CU1	Pattern	Levels/Edges/Comparisons	NO	Disabled	1024	3	16	Clk
CU2	Video	Levels/Edges/Comparisons	NO	Disabled	2048	2	46	vid Clk
CU3	Video-	Levels/Edges	NO	Disabled	1024	1	80	vid Clk
	Extended							-

Capture	Data	Nodes	Data	Trigger
Unit	group			
CU1	Cnt	g_demo[0].u_core/Cnt[150]	YES	YES
'Pattern'	Sine	g_demo[0].u_core/sine_Data[150]	YES	YES
	Noise	g_demo[0].u_core/Rnd[150]	YES	YES
CU2 'Video'	SDI	g_demo[0].u_core/sdi_SOF	YES	YES
		g_demo[0].u_core/sdi_VBlank	YES	YES
		g_demo[0].u_core/sdi_HBlank	YES	YES
		g_demo[0].u_core/sdi_Valid	YES	YES
		g_demo[0].u_core/sdi_LN[110]	YES	YES
		g_demo[0].u_core/sdi_R[90]	YES	NO
		g_demo[0].u_core/sdi_G[90]	YES	NO
		g_demo[0].u_core/sdi_B[90]	YES	NO
	Noise	g_demo[0].u_core/vid_Sine[150]	YES	YES
		g_demo[0].u_core/vid_Noise[170]	YES	NO
		g_demo[0].u_core/vid_Addr[90]	YES	NO
CU3 'Video-	Vid-	g_demo[0].u_core/sdi_SOF	YES	YES
Extended'	Extended	g_demo[0].u_core/sdi_VBlank		YES
		g_demo[0].u_core/sdi_HBlank		YES
		g_demo[0].u_core/sdi_Valid		YES
		g_demo[0].u_core/sdi_LN[110]		YES
		g_demo[0].u_core/sdi_R[90]		NO
		g_demo[0].u_core/sdi_G[90]		NO



	g_demo[0].u_core/sdi_B[90]	NO
	g_demo[0].u_core/vid_Sine[150]	NO
	g_demo[0].u_core/vid_Noise[170]	NO
		_

✓ CAPTURE CONFIGURATION: DONE !

(! Don't forget to save your project !)

Step 3: Run Insertion

This part of the flow executes the following:

- IP configuration checks
- EXOSTIV IP synthesis with Vivado
- EXOSTIV IP insertion in the target FPGA netlist
- Additional constraints generation
- Instrumented design implementation and bitstream generation.

	wproject.epf							_		
alp										
. . .										
Link	2 2	Capture Configuration	2.2	2	Insert EXOSTIV IP	Σ	2 2	Debug Design	l 1	
	do/2016 2/bio	Use this but	tton to sta	Output	eneration an	d insertio	n proce	255		
Manage Cach	e	~		EXOSTIVIT INSC						
- Counting										_
de shell	The path to t	the Vivado ex	ecutable i	must be sp	ecified					
do snell	before starti	ing the IP gen	eration/in	sertion.		-				
dag core project						-				
debug core					Specify t	- ne name o	the F	(OSTIV IP ins	ance	
debug core					Speenyt	ic name c	in the Ly		lance	
nrohes						-				
onstraints										
check						-				
nt design impl_1		•				-				
rate bitstream										
										-
rate bitstream				•						

- 2. Enable Implementation and select 'impl_1' from the drop down list: Select 'Implement Design' and 'Generate bitstream'.
- 3. Click on 'Insert EXOSTIV IP' button.

Insertion running ... and completed.



Leels Hele	13 ON/Demo Wiek 5	links/demo_mica702-3	inks.epi				_	
Link Configuration	2 2	Capture Configuration	> >		Insert XOSTIV IP	>>>	Debug Design	
	ha da							
Cancel Insertion								
Configuration				Output				
/ivado installation folder C:/cad/Xilinx/Vivado/2016	.2/bin			EXOSTIV IP instance nam	e exi_top			
Checking configuration						Done (0:00:02)		
Starting Vivado shell						Done (0:00:07)		
Creating debug core project						Done (0:00:01)		
Configuring debug core						Done (0:00:00)		
Generating memories						0:00:00		
Synthesising debug core						-		
Inserting debug core								
Connecting probes						-		
Generating constraints								
Design rules check	-					-		
✓ Implement design impl_1	•					-		
✓ Generate bitstream								
INFO: [IP Flow 19-234] Refreshing IP repositories			Log W	indow				
INFO: [IP_Flow 19-1704] No user IP repositories s	pecified							
flow 🛛 Vivado link 🖌 🗍 EXOSTIV Probe 💥 🗍 FF	PGA link X							
Iools Help								
Link	>>	Capture			Insert	>>>	Debug	
Link Configuration	2 2	Capture Configuration	> >		Insert (OSTIV IP	>>>	Debug Design	
Link Configuration	<u>}</u>	Capture Configuration	> >		Insert (OSTIV IP	>>>	Debug Design	
Link Configuration	>>	Capture Configuration	> >	Output	Insert KOSTIV IP	>>>	Debug Design	
Link Configuration Insert EXOSTIV IP anfiguration vado installation folder [C:/cad/xilmx/Vivado/Z016	> >	Capture Configuration	> >	Output EXOSTIV IP instance nam	Insert (OSTIV IP	>>>	Debug Design	
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Link Configuration Insert EXOSTIV IP Infiguration vado installation folder C:/cad/Xilinx/Vivado/2016 se IP cache IP cache ogress	> > [Capture Configuration		Output EXOSTIV IP instance nam	Insert COSTIV IP	>>>	Debug Design	
Link Configuration	> >	Capture Configuration		Output EXOSTIV IP instance nam	Insert (OSTIV IP e exi_top	Done (0:00:02)	Debug Design	
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Link Configuration	> >	Capture Configuration	/ Dashboard mplementation	Output EXOSTIV IP instance nam	Insert (OSTIV IP e exi_top	Done (0:00:02) Done (0:00:07) Done (0:00:07) Done (0:00:01) Done (0:00:03) Done (0:00:39) Done (0:00:59) Done (0:00:13) Done (0:00:13) Done (0:00:19) Done (0:00:19)	Debug Design	
Link Configuration	> >	Capture Configuration	/ Dashboard mplementation	Output EXOSTIV IP instance nam	Insert (OSTIV IP e exi_top	Done (0:00:02) Done (0:00:07) Done (0:00:07) Done (0:00:01) Done (0:00:03) Done (0:00:359) Done (0:00:13) Done (0:00:55) Done (0:00:19) Done (0:00:19) Done (0:00:19)	Debug Design	
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Link Configuration Insert EXOSTIV IP infiguration Vado installation folder C:/cad/Xilmx/Vivado/2016 Ise IP cache Ingress Checking configuration Starting Vivado shell Creating debug core project Configuring debug core Generating debug core Inserting constraints Design rules check Implement design impl_1 Implement design Implemen	> >	Capture Configuration	/ Dashboard mplementation	Output EXOSTIV IP instance nam	e exi_top	Done (0:00:02) Done (0:00:02) Done (0:00:07) Done (0:00:01) Done (0:00:03) Done (0:00:359) Done (0:00:13) Done (0:00:55) Done (0:00:19) Done (0:00:19) Done (0:00:14)	Debug Design	
Link Configuration	> > >	Capture Configuration	/ Dashboard mplementation	Output EXOSTIV IP instance nam	e exi_top	Done (0:00:02) Done (0:00:07) Done (0:00:07) Done (0:00:01) Done (0:00:03) Done (0:00:13) Done (0:00:13) Done (0:00:19) Done (0:00:03) Done (0:00:03) Done (0:00:03) Done (0:00:03) Done (0:00:03)	Debug Design	
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Link Configuration Insert EXOSTIV IP anfiguration vado installation folder C:/cad/klinx/Nivado/2016 se IP cache Manage Cache ogress Checking configuration Starting Vivado shell Creating debug core project Configuring debug core Generating memories Synthesising debug core Connecting probes Generating constraints Design rules check Implement design impl_1 Generate bitstream	> > > [Capture Configuration	/ Dashboard mplementation	Output EXOSTIV IP instance nam	Insert (OSTIV IP e exi_top	Done (0:00:02) Done (0:00:07) Done (0:00:07) Done (0:00:03) Done (0:00:03) Done (0:00:03) Done (0:00:05) Done (0:00:05) Done (0:00:19) Done (0:00:19) Done (0:00:19) Done (0:00:14)	Debug Design	
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Click on 'OK' at prompt to save the project.

Auto Save Project	\times
The project file must be saved when EXOSTIV IP is inserted. This ensures a project file is uniquely linked to the inserted IP.	
Automatically save the project file.	
Cancel OK	

We can check that 'exi_top' was inserted into the design if you open the 'design implementation' in Vivado (Don't save when prompted to save synthesized design):





demo_03 - [P:/Xplorer/hardware/fpga/DEMO_MIC_A7_02 - export/impl/demo_03/demo_03.xpr] - Vivado 2016.2
 File Ent Flow Tools Window Lawout View Help

File Edit Flow Tools Window Layout View Help		Q.→ Search commands
😂 🖿 i 🗠 🕶 🐂 🐂 🗙 🛷 i 🔈 🎽 🖄 🏈	🗘 🥝 🊳 🐝 🔽 🞼 🖳 Default Layout 💿 👻 🎇 🐂 🔳 🖏	write_bitstream Complete
Flow Navigator ? «	Implemented Design - impl_1 xc7a35tcsg325-2 (active)	? ×
९ 🔀 🖨	Netlist ? = 🗆 🗠 × 💽 Project Summary 🗙 🛞 Device 🗙 🔄 Schematic (2) :	< ? 🗆 🕹 ×
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 ✓ Synthesis Image: Synthesis Settings ✓ Run Synthesis ✓ E Synthesized Design ▲ Constraints Wizard 	Name: exi_top Reference name: exi_top Type: Others Number of indice: 24 General Properties Statistics Nets Cell Pins Children	OBUF OBUF OBUF OBUF OBUF
Edit Timing Constraints Set Up Debug Ø Report Timing Summary By Report Clock Networks Report Clock Interaction P. Deport Mathematican V	Timing Summary - impl_1 Inter-Clock Paths Timing Summary - impl_1 Timing Summary - impl_1 Inter-Clock Paths	

Program the target board

We now need to use the generated binary to program the target board.

- Return to Vivado and open the 'Hardware Manager'.
- Connect the programming cable to the MICA board
- Turn on the MICA board by enabling the output HDMI power and connecting to the EXOSTIV Probe.
- Once connected, right-click on the target FPGA and select 'Program'.
- Then, select the generated bit file and load the FPGA configuration.





Creating a 'RTL flow' project with EXOSTIV Dashboard

The 'RTL flow' enables configuring and synthesizing EXOSTIV IP for insertion in RTL source code. The 'RTL flow' is somewhat simpler than the 'netlist flow' as it does not involve user interactions with Vivado. EXOSTIV IP is inserted and connected to the target FPGA design nodes by instantiating EXOSTIV IP in the RTL code – a 'manual' process.

1. From the Welcome screen, click on 'Create New Project' The 'Create New Project' window appears, prompting to select the desired flow (Netlist flow or RTL flow). Specify a project name and pick a location. The 'Link Configuration window' of the core inserter appears. EXOSTIV Dashboard × <u>File Tools H</u>elp 🗟 📄 🖬 🛃 🔌 😤 🗰 EXOSTIV[™] Reach. Store. Analyze. FPGA Debug Reloaded Create New Project User Guide / Getting Started A wizard will help you create a new Detailed information about EXOSTIV. project Open Project Knowledge Base Open an existing project. Online knowledge base. Open Recent Project Open an recently used project. lanage licenses. 🔲 New Project ? × Create New Project **RTL IP insertion** • Type The EXOSTIV IP is configured and synthesized based on the number of nodes to be connected from the target FPGA design. EXOSTIV IP is synthesized and provided as a netlist and a RTL component / module. The target RTL code must be manually edited to insert and connect the EXOSTIV IP. new_project Name Create in C:/Users/frederic Browse... Cancel Create



EXOSTIV Dashboard for Xilinx - C:/Users/frede/new_pr	oject.epf	– 🗆 X
💽 📴 🛄 📓 🕺 💥 🕷		
Link Configuration	Capture Configuration Capture Configuration	Debug Design
FPGA Type	Connector	
Family Artix-7 - Defense-grade 🔻	Connector type HDMI	
Package cs325 💌		
Speed grade -1I 💌		
Part xq7a50tcs325-11		
Upstream Link	Downstream Link	
Transceiver bank 216	Use I2C link	
MGT type GTP	SCL package pin A9	
MGT_TxP0 H2	SDA package pin A9	
MGT_TxP1 F2	SCL I/O standard LVCMOS33 👻	
MGT_TxP2	SDA I/O standard LVCMOS33 🔹	
MGT_TxP3 B2		
Reference Clock		
Iransceiver bank 216		
Frequency (MHz) 100		
Range ; 60 MHz to 660 MHz		
Line rate (Gb/s) 3.2 🔻		
Link rate (Gb/s) 0		
PLL type used QPLL EXOSTIV dock output		
	Log Window	
g Info : Project file "D:/Projects/Xplorer/Hands-On/Demo-MIC	A-3links_1.8.x/demo_mica702-3links-1.8.2.epf" loaded successfully.]
Info : Project file "C:/Users/frede/new_project.epf" written	successfully.	
sole		
ē		
RTL flow Vivado link 🗱 EXOSTIV Probe 💥 FPGA link 💲	¢	

Using the IP generator (RTL flow)

In RTL flow, the EXOSTIV Dashboard allows to generate EXOSTIV IP. Unlike the 'netlist flow', RTL flow won't automatically insert EXOSTIV IP into the target design. This has to be done 'manually', in the RTL code (VHDL / Verilog).

Generating EXOSTIV IP in RTL flow requires 3 steps:

- Step 1 : Link Configuration
- Step 2 : Capture Configuration
- Step 3 : Generate EXOSTIV IP

These 3 steps are accessible through the top flow overview in the EXOSTIV Dashboard window





Step 1: Link Configuration

This step in RTL flow does not differ from the same step in netlist flow. Please refer to Step 1: Link Configuration, page 23 for an illustrated example on how to use it.

Step 2 : Capture Configuration

During this step, the characteristics of EXOSTIV IP are defined:

- Capture units
 - o Number and names
 - Trigger options
 - $\circ \quad \ \ \text{Size of the memory buffer}$

- Data groups

- Number and names
- As opposed to the 'netlist flow' described at page (-), data group definition is limited to:
 - The number of bits in each data group
 - The quality of the inputs of each data group: the number of 'data / trigger' nodes and the number of 'data only' nodes.

Capture units (3 out of max. 16)		Pattern		
Y Pattern	Triggering		Data	
Sine	Trigger unit type	Levels / Edges / Comparisons	Fifo depth	1024 👻
Cnt	Bit operations	X, 0, 1, R, F, B, N	Number of data groups	3 out of max 16
Rnd	Bus operations	==, >, <, >=, <=, <>, in range, out of range		
Double click to add Data Group	Counter width	Disabled 👻	Number of data probes	16 out of max. 2048
✓ Video	Sequencer Depth	Disabled	Number of data only probes	0 out of 16
SDI	Storage qualification			
Noisy Sine	Number of pipes	Disabled 👻		
Double click to add Data Group				
✓ Video-ext				
Data Group 1				
Double click to add Data Group				
Double click to add Capture Unit	•			

Use this panel to define the Capture units and the data groups.



Control control control control control consigned of the product of the p	EXOSTIV Dachboard - Cr/Projects/Xplorer/b	Hands-On/RTUP/DebugCoreTor) enf				×
Ide José Beép Ide	Exos in Dashboard - C./Projects/Apiorei/I	ands-On/RELE/DebugColeTop	лері				~
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Unk >>>> Capture >>>>>>>>>>>>>>>>>>>>>>>>>>>>>>							
Capture units (soutofmax. 16) Pattern Site Image: init type Levels / Edges / Comparisons Data Note Rod Bas operations Rod, R. F.B. N Duble dok to add Data Group Welce Storage qualifaction Data V Welce Soit Bas operations Trigger unit type New of data groups V Welce Soit Bas operations Trigger unit type New of data groups V Welce Data Group Storage qualifaction Data Data of data Group Data Group 1 Data Group 1 Data Group 1 Double dok to add Data Group Use this panel to define the capture units and the data groups. For each capture unit, define: Use this panel to define the capture units and the data groups. The number of data probes Optionally, the number of data probes Optionally, the number of data probes Optionally, the number of data probes Optionally, the number of data probes The data groups. The number of data probes Optionally, the number of data probes The data groups. The number of data probes Optionally, the number of data probes The data groups. The supering free dore data dore data data data data data data data dat	Link Configuration	Capture Configuration	>>>	Generate EXOSTIV IP	<u>>>></u>	Debug Design	
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Step 3 : Generate EXOSTIV IP

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Overview of the files generated with the RTL flow

A series of files are generated by the EXOSTIV Dashboard RTL flow IP generation process. These files must be used with the target FPGA design in order to instrument the target FPGA and use EXOSTIV to debug the FPGA.

All the files names are prefixed with the EXOSTIV IP instance name specified in the project. Here is the list of generated files and their usage:

File name	Usage	Add to Vivado project?						
<instance name="">.edf</instance>	EXOSTIV IP synthesized netlist.	YES						
<instance name="">.vhd</instance>	Example template on how to instantiate the EXOSTIV IP in the target design	NO this is an example template.						
<instance name="">_pinout.xdc</instance>	Constraint file containing the pinout required by the EXOSTIV IP (like transceiver location).	YES						
<instance name="">_pkg.vhd</instance>	VHDL Package file containing types used for the EXOSTIV IP instantiation.	YES						
<instance name="">_timing.xdc</instance>	Constraint file containing the timing constraints relative to EXOSTIV IP.	NO, should be 'sourced' in Vivado, not just added.						

RTL flow: inserting EXOSTIV IP and implementing the design

From here, the RTL code of the target design has to be modified manually. An instance of EXOSTIV IP has to be created. The connection with the design internal nodes should be done at this step, from the RTL code.

Then the required files should be added to the Vivado project and the synthesis / implementation / bitstream generation of the instrumented design can be run from the Vivado interface.

Finally, the bitstream has to be used with the target board, and EXOSTIV analyzer can be used for extracting trace data (refer to page 12).



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