EXOSTIV™

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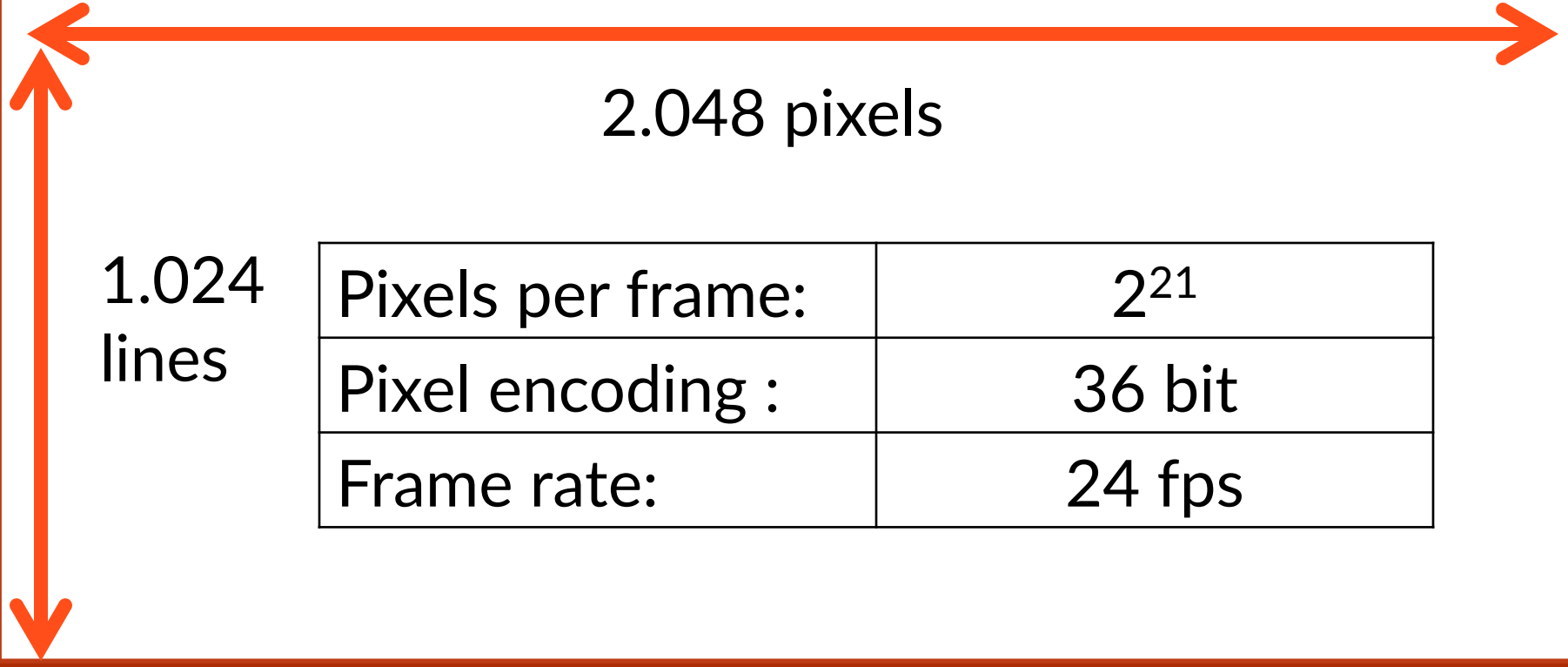
EXOSTIV LABS

A simple case: a video processing platform

Headers & controls per frame : 1.024 bits



Pixels per frame:	2^{21}
Pixel encoding :	36 bit
Frame rate:	24 fps

‘Something’ goes wrong…

- Randomly
- Unknown time from cause to effect
- Occurs when system is put together
- Not everything was designed in-house

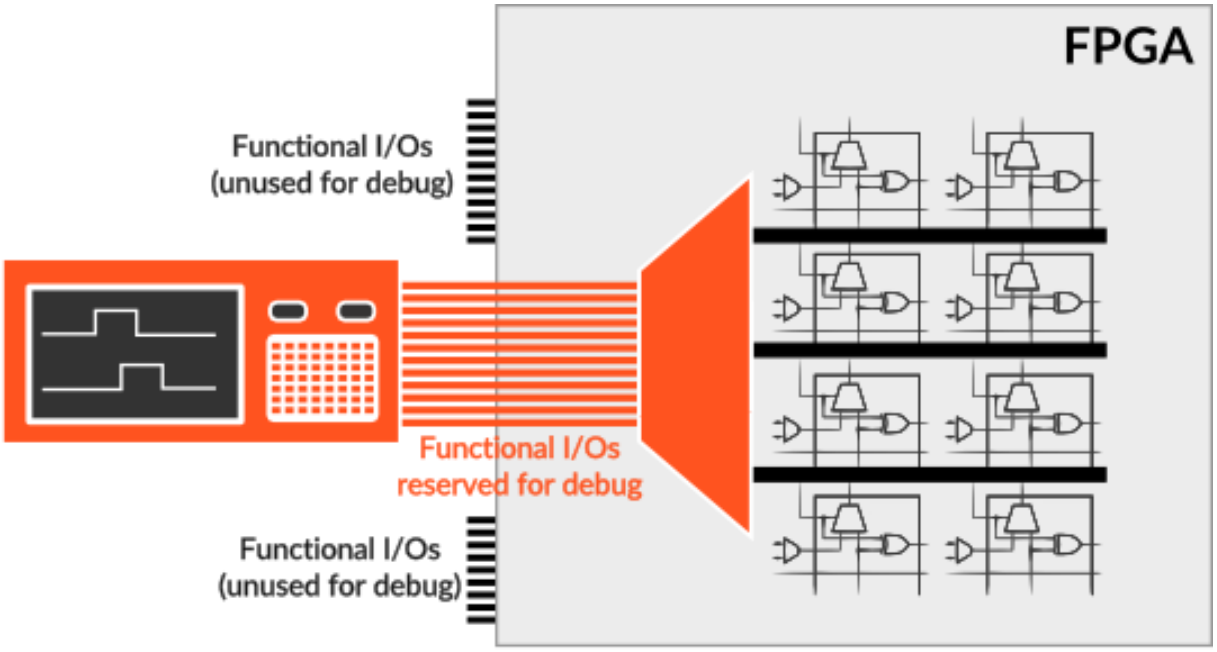
Typical debug case

- **‘Emergent system’** type: function of not just the individual little pieces, but the *way they collectively interact as a whole*.

- **‘Some’ history’** must be captured.
  We don’t know how much of that history is necessary

- **Simulation-only cannot be used:**
  - too long to be practical
  - there is probably a problem of modelling since the bug was not detected during RTL verification.
  - we need to ‘narrow in’ on the bug first

Debugging with a ‘traditional’ LA



Debugging with a 'traditional' LA

1) Is there any usable connector on the FPGA I/Os?
   In our case : no connector → we cannot use a LA.

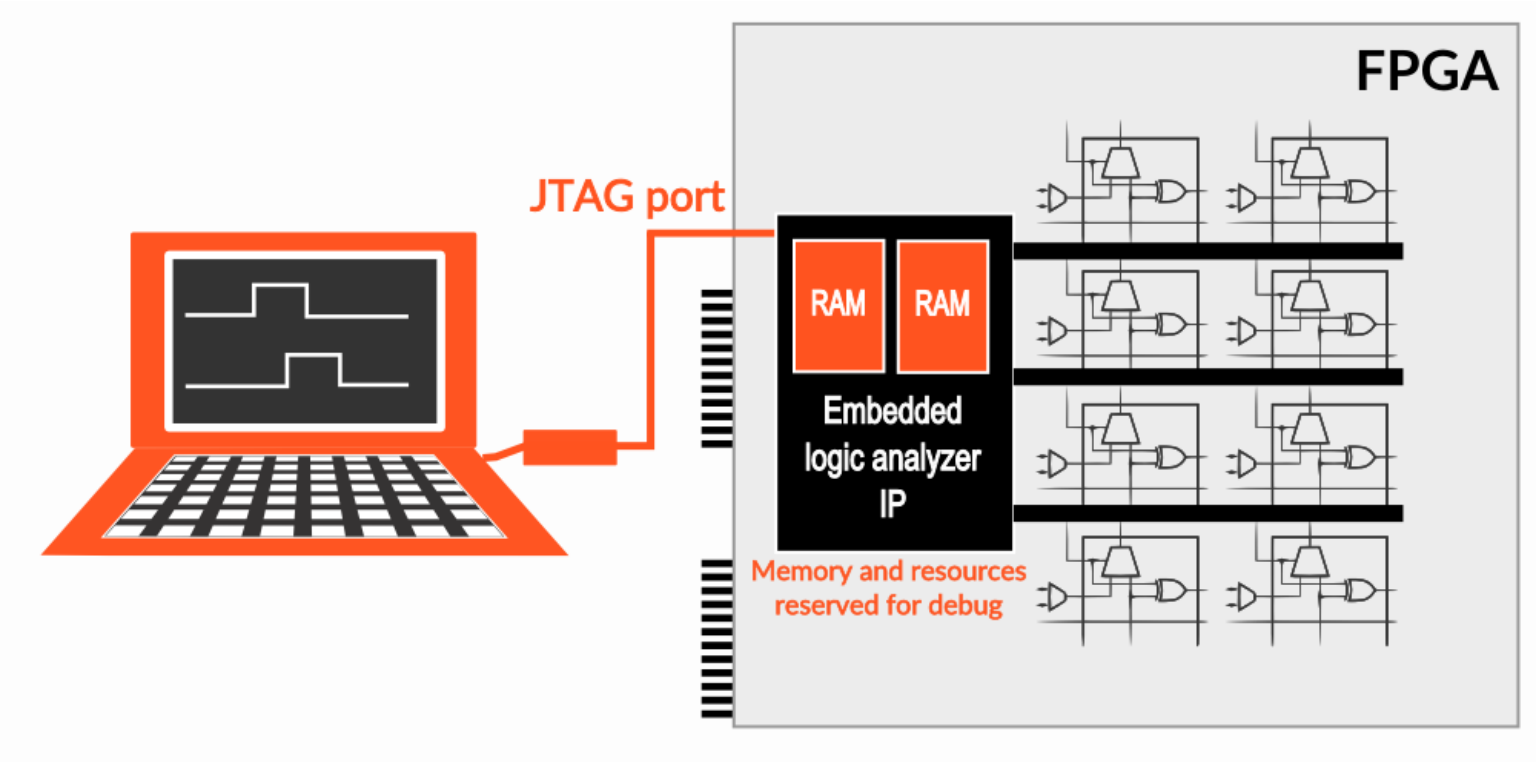
Supposing there is a connector…

2) Can the interesting signals be routed 'as is'?
   - Sampling speed: 200 MHz to 400 MHz. Can the I/O do it?
   - Can the PCB support that speed?
   - There aren't probably enough pins

3) Does the design need to be adapted?
   - Data buffering + clock speed adaptation
   - Time-multiplexing on the available debug I/Os

Question: How can you foresee the required 'real estate' when you don't know what you'll have to debug?

Debugging with an Embedded LA



Debugging with an Embedded LA

1) Limit capture to header and controls : **1.024 bit per frame**
2) Worst case : full 2 hours movie at 24 fps:

1.024 b x 2 h x 3.600 s x 24 fps = 176.947.200 b ~ **22 MB**

3) Reality: 32 kbit RAM is available for debug in the FPGA.
   = Debug information for 32 frames
   ➔Equivalent to 1,33 s of a 2 hours movie.

'Shooting in the dark'?

4) Solution: we need a more clever triggering approach…

Question: how do you trigger on something you *do not know*?

What is EXOSTIV™?

- EXOSTIV is a new kind of **embedded instrument for FPGA debugging**
- EXOSTIV uses a **dedicated hardware** with **high bandwidth** and **large storage capacity** to reach very large observability levels on FPGA during **in-lab testing.**

Debug & Verification

‘Pure’ Software	Emulation & Hardware Acceleration	Prototype board & Target board EXOSTIV

Problem

Due to FPGA complexity, **Debugging & Verification times Increase**

Today's solutions

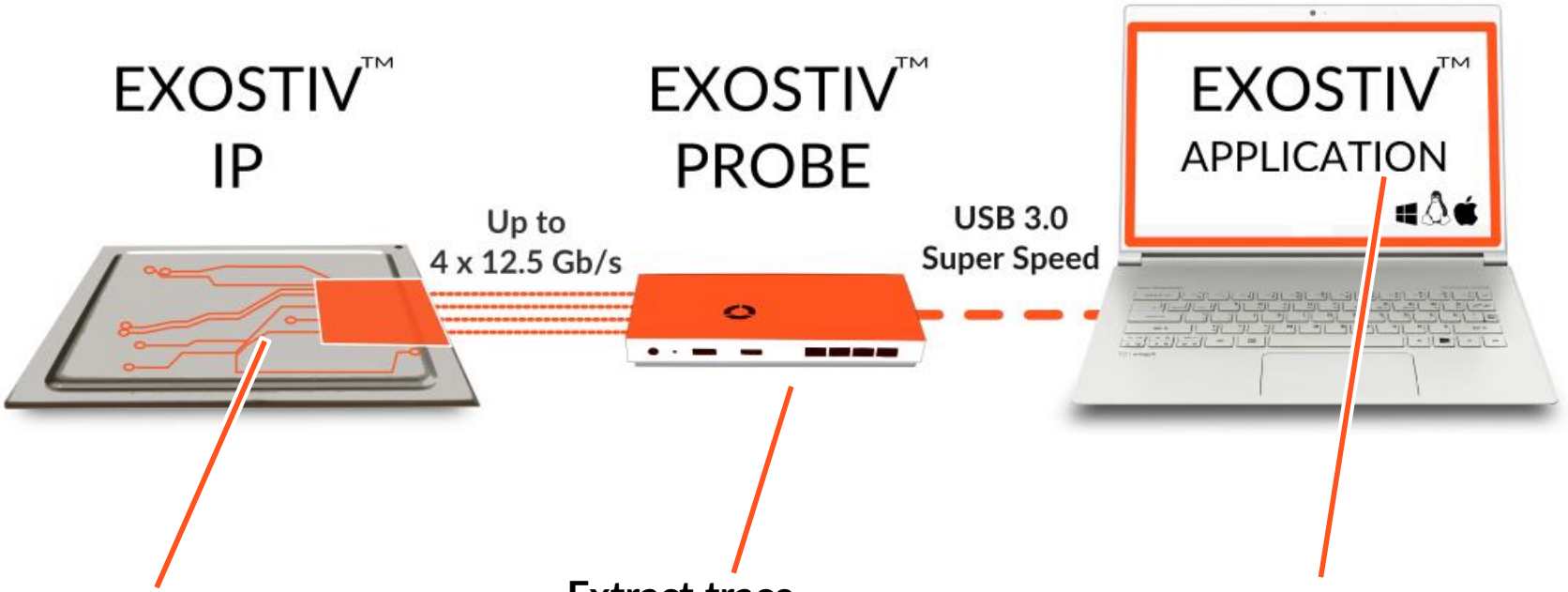
1. RTL Simulation (SW only) Long runtime !
2. 'Embedded LA' Chipscope / SignalTap (in-lab)
   Available FPGA memory
3. Logic Analyzer / Scope (in-lab)
   - Available I/Os
   - Limited width
   - Board issues with parallel bus
   - At speed sampling...?

New solution

EXOSTIV = embedded instrument

1. Transceivers (MGT) ~~JTAG~~
2. Deep external memory
3. At speed (sampling & execution)
4. Analysis tools for (very) large traces

EXOSTIV™ - Overview



Reach internal nodes

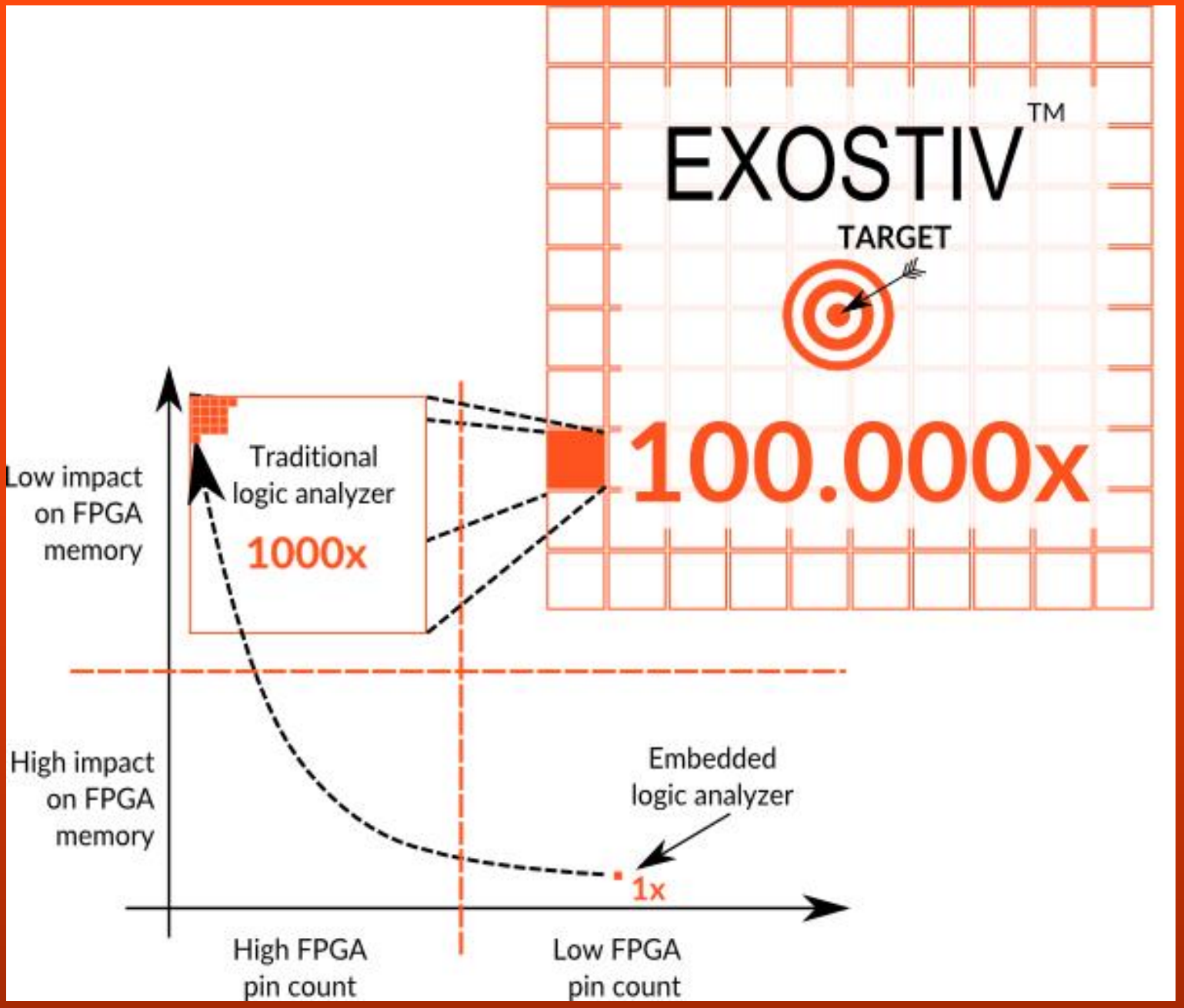
- Up to **16 capture units**
- Up to **16 data sets** per CU
- **1 trigger + 1 qualification unit** per CU
- Up to **2.048 nets** per data set
- IP RAM does not grow with capture size
- Sampling **@ system speed**

Extract trace

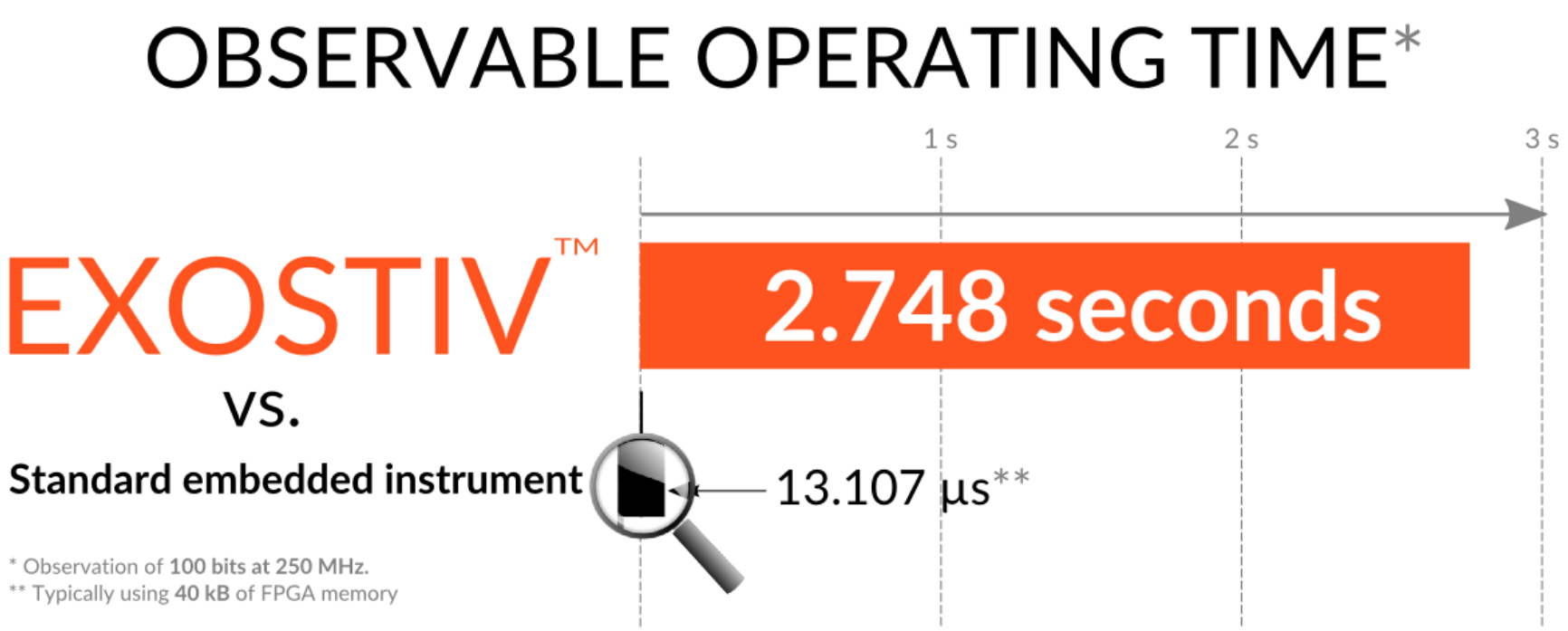
- Up to **8 GB** for trace storage
- Up to **4 x 12.5 Gbps** bandwidth
- Uses **Multi Gigabit Transceivers**
- **HDMI** and **SFP+** cage connector
- Optional connector adapters
- Downstream channel for IP control
- **USB 3.0** connection with workstation

Control & Analyze

- IP configuration & insertion
- Trigger and data filter set up
- IP communication and control
- Trace reception and encoding
- Advanced waveform viewer


EXOSTIV™
TARGET
100.000x
Traditional
logic analyzer
1000x
Low impact
on FPGA
memory
High impact
on FPGA
memory
Embedded
logic analyzer
1x
High FPGA
pin count
Low FPGA
pin count

Indicative gain



EXOSTIV™ - Probe

Power button

Extra downstream control connector

High-speed connector – HDMI format – up to 4 x 6.6 Gbps

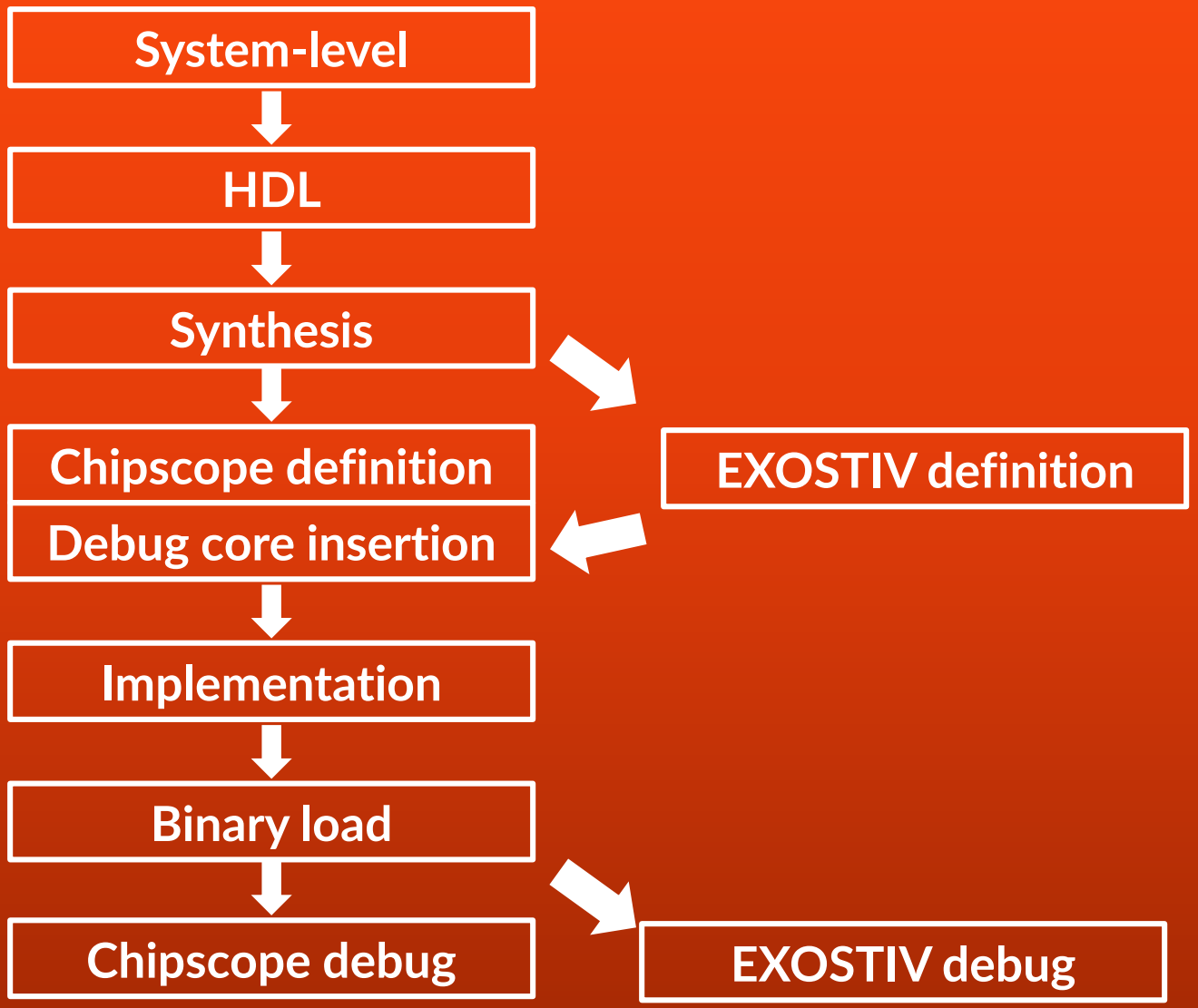
Status LED

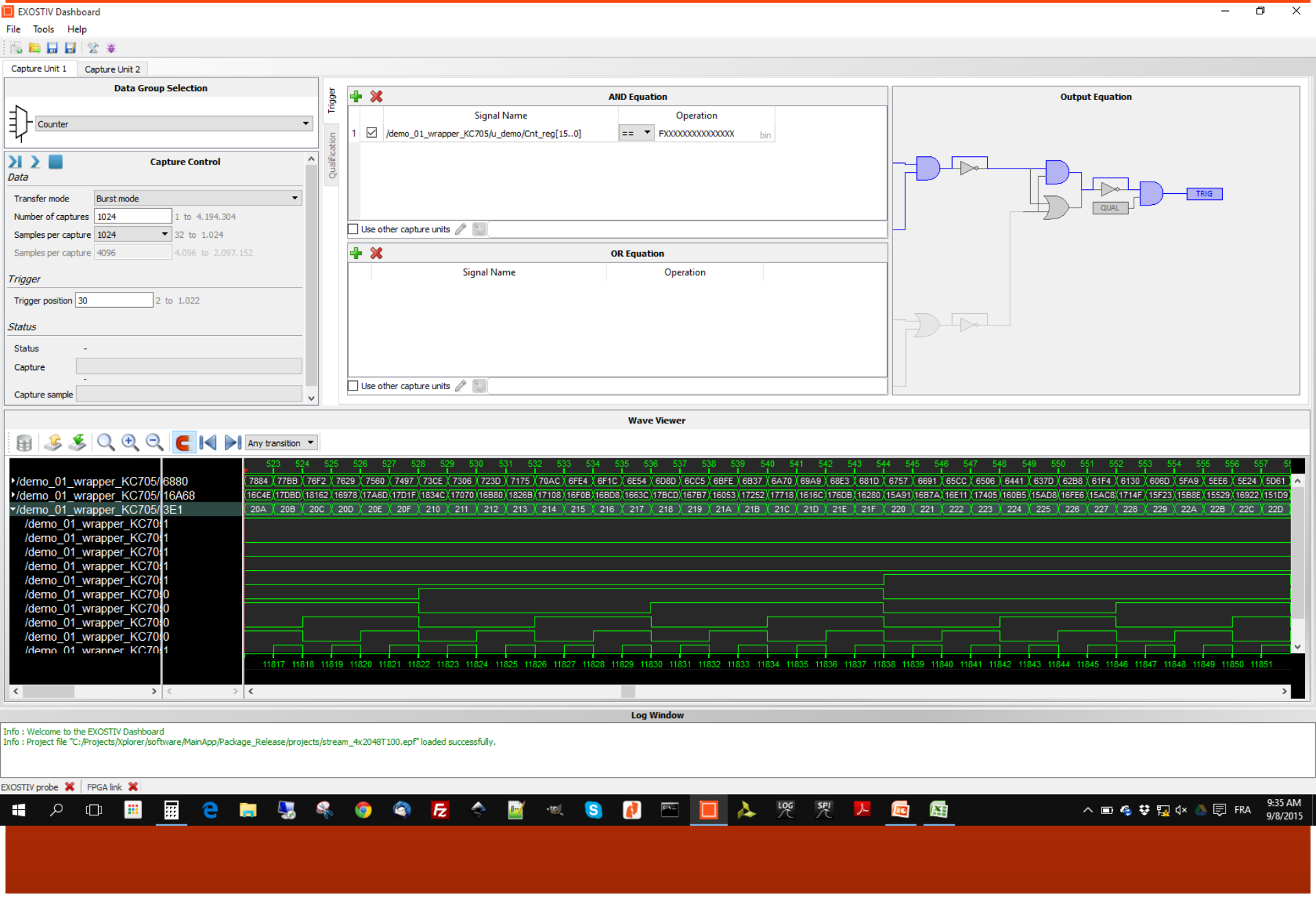
High-speed connector – SFP+ format – up to 4 x 6.6 Gbps

USB 3.0

DC power jack

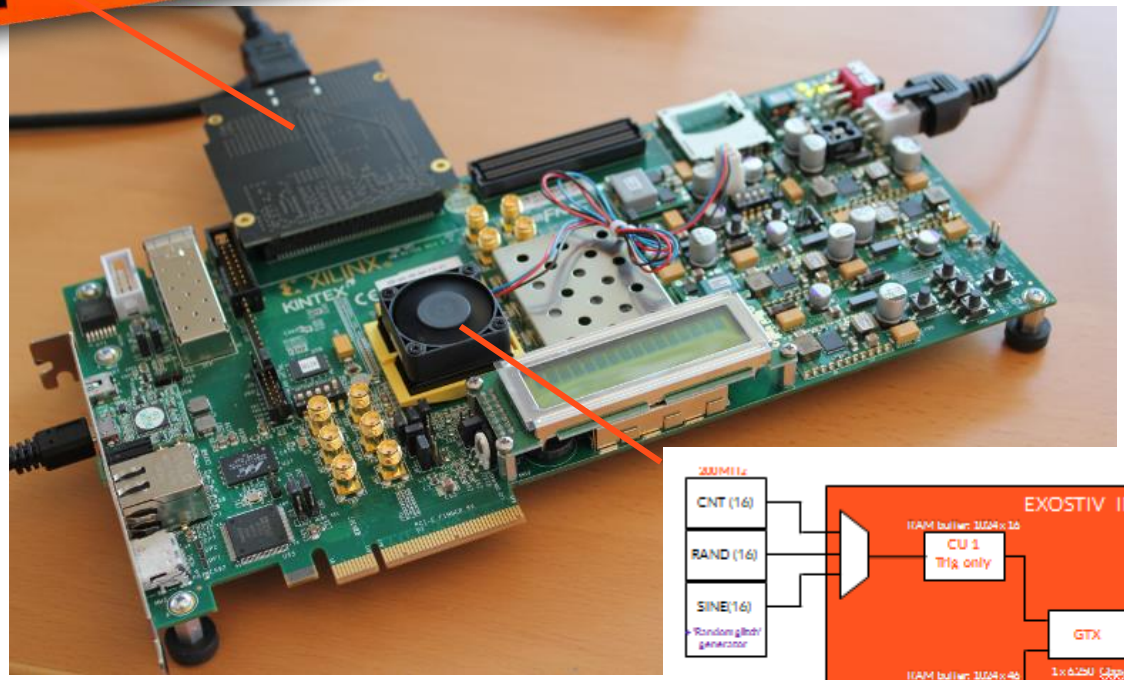
EXOSTIV™ in Vivado flow




EXOSTIV Dashboard
File Tools Help
Capture Unit 1
Capture Unit 2
Data Group Selection
Counter
Capture Control
Data
Transfer mode
Burst mode
Number of captures
1024
1 to 4.194.304
Samples per capture
1024
32 to 1.024
Samples per capture
4096
4.096 to 2.097.152
Trigger
Trigger position
30
2 to 1.022
Status
Status
Capture
Capture sample
Trigger
Qualification
AND Equation
Signal Name
Operation
1
/demo_01_wrapper_KC705/u_demo/Cnt_reg[15..0]
==
FXXXXXXXXXXXXXXX
bin
Use other capture units
OR Equation
Signal Name
Operation
Use other capture units
Output Equation
TRIG
QUAL
Wave Viewer
Any transition
/demo_01_wrapper_KC705/6880
/demo_01_wrapper_KC705/16A68
/demo_01_wrapper_KC705/3E1
/demo_01_wrapper_KC705/1
/demo_01_wrapper_KC705/1
/demo_01_wrapper_KC705/1
/demo_01_wrapper_KC705/1
/demo_01_wrapper_KC705/1
/demo_01_wrapper_KC705/0
/demo_01_wrapper_KC705/0
/demo_01_wrapper_KC705/0
/demo_01_wrapper_KC705/0
/demo_01_wrapper_KC705/1
Log Window
Info : Welcome to the EXOSTIV Dashboard
Info : Project file "C:/Projects/Xplorer/software/MainApp/Package_Release/projects/stream_4x2048T100.epf" loaded successfully.
EXOSTIV probe
FPGA link
FRA
9:35 AM
9/8/2015

Demo – Overview (1)

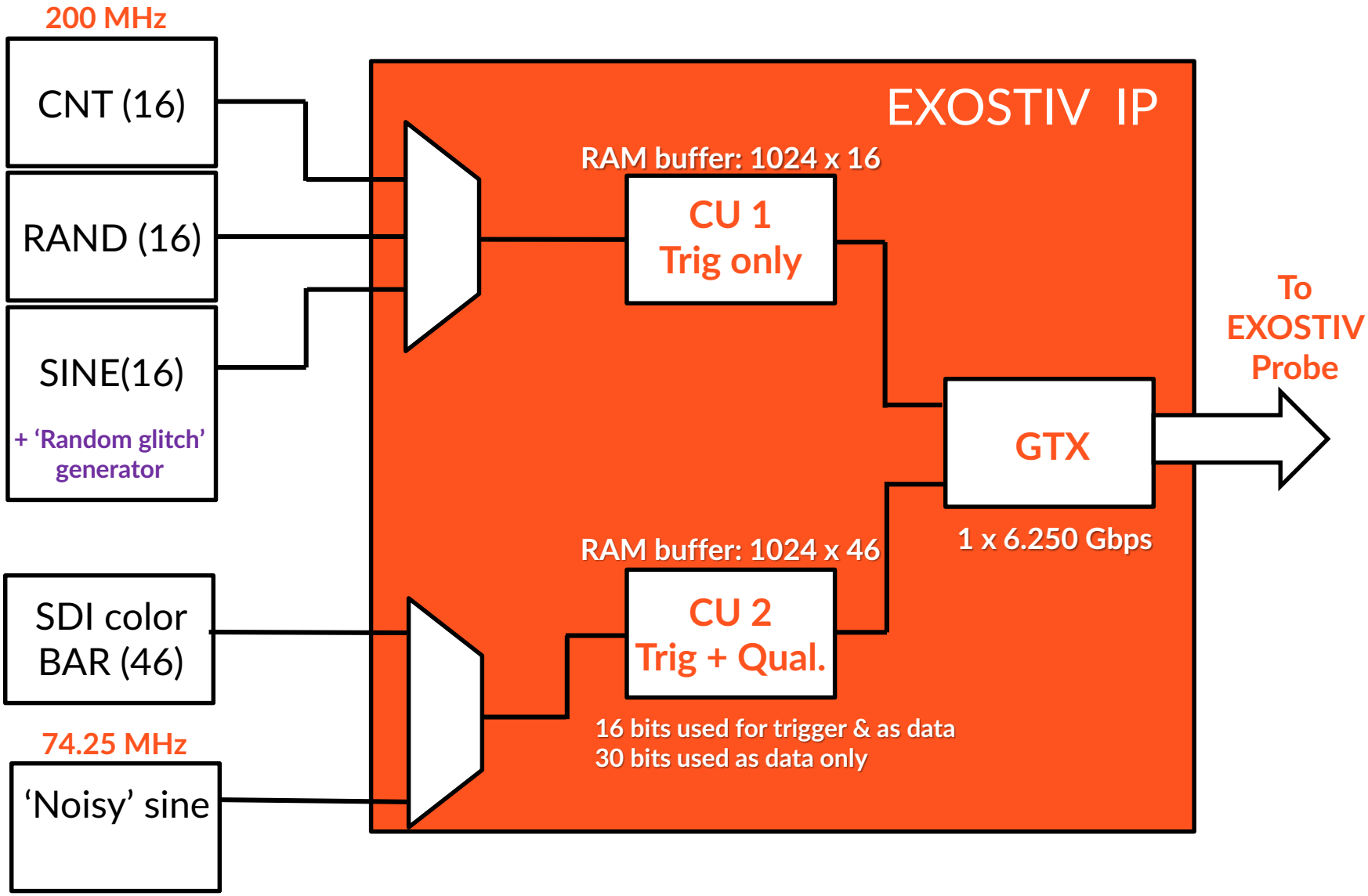
Connection with EXOSTIV Probe
FMC connector + Adapter → HDMI input



Xilinx Kintex-7 evaluation kit

Demo design + EXOSTIV IP in Kintex-7

Demo – Detail of design & IP



Thank you -
Any questions?

FPGA Debug Reloaded

www.exostivlabs.com