# EXOSTIV

# Using the KCU105 Kintex Ultrascale evaluation kit

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# References

# **Revision History**

| Revision | Modifications  |  |  |  |  |
|----------|--|--|--|--|--|
| 1.0.0    | Initial revision   |  |  |  |  |
| 1.0.1    | Added FMC HPC support  |  |  |  |  |
| 1.0.2    | <ul> <li>Pinout correction for the HDMI interface</li> <li>Corrected clock frequency for the transceivers in HDMI mode to 125 MHz</li> </ul> |  |  |  |  |
| 1.0.3    | Review and update for EXOSTIV Dashboard v. 1.8.2 release   |  |  |  |  |



# EXOSTIV – using the KCU105 kit

### Introduction

This document provides information about using EXOSTIV with the KCU105 Kintex Ultrascale evaluation kit (<u>http://www.xilinx.com/products/boards-and-kits/kcu105.html#overview</u>).

# Using EXOSTIV with KCU105 evaluation kit through SFP+

EXOSTIV can be connected to the KCU105 evaluation kit through the SFP / SFP+ connectors with direct SFP cables or through another connector (e.g. the FMC HPC or FMC LPC connectors), possibly with an adapter.

In this document, we'll describe how to use EXOSTIV with the KCU105 kit SFP/SFP+ connector. We provide several .epf files to be used with the EXOSTIV Dashboard, that are pre-configured for use with 1 or 2 of the board SFP ports.

#### **KCU105** : overview





#### **Connecting the KCU105**

- 1) For Data: 1 or 2 SFP cables can be used:
  - a. When using 1 SFP connection, plug it into SFP0 of KCU105 on one end and any of the SFP ports of the EXOSTIV probe (S0, S1, S2 or S3). Use EPF file '**KCU105-1SFP-link.epf**' with EXOSTIV Dashboard.
  - b. When using 2 SFP connections, plug one cable into each of the SFP ports of the KCU105 and the 2 cable's other end to any of the SFP ports of EXOSTIV Probe. Use EPF file 'KCU105-2SFP-links' with EXOSTIV Dashboard.
- 2) For the SFP reference clock: KCU105 does not provide any on-board oscillator directly attached to the SFP port. This clock must be supplied through one of the board connectors. In the example, we have chosen to generate the clock with the EXOSTIV Probe and connect it to the KCU105 board with the SMA clock connector.

 $\rightarrow$  Connect a pair a SMA cables into the GTH reference clock input SMA connector of the KCU105 board (see picture above) and the other end into the clock output port of the EXOSTIV Probe. The .epf files are set up so the clock is generated with the EXOSTIV Probe.

#### **Reviewing the .epf files settings**

In the provided .epf files, only the 'link configuration' is set up:

#### 'KCU105-1SFP-link.epf' :

| E                                | P-link.epf — 🗆 X  |   |
|----------------------------------|---|---|
| Kintey Ultrascale part           | Link<br>Configuration         Capture<br>Configuration           FPGA Type         Family           Family         Kintex UltraScale  | Run   Debug     Insertion   Design       Connector     Connector type       SFP   |
| mounted on the KCU105<br>board   | Package ffva1156<br>Speed-grade -2<br>Part xcku040-ffva1156-2-e   | We use the SFP connector type on the EXOSTIV Probe.   |
|                                  | Upstream Link<br>Transceiver bank 226   | Downstream Link O Use I2C link  Use transceiver link  |
|                                  | MGT type         GTH           MGT_TxP0         AA4           MGT_TxP1         W4           MGT_TxP2         U4           MGT_TxP3         R4   | Transceiver bank       226         MGT_RxP0       Y2         MGT_RxP1       V2         MGT_RxP2       T2         MGT_RxP3       P2    We use SFP0 on the KCU105 board. The Tx and Rx P pins of the SFP0 are connected to U4 and T2 pins respectively (bank 226) |
|                                  | Reference Clock Transceiver bank 226 MGT_REFCLK_P0 V6 MGT_REFCLK_P1 T6 Frequency (MHz) 132  | Location of the SMA reference clock P<br>pin on the FPGA package. Pin V6, bank<br>226   |
|                                  | Range : 60 MHz to 280 MHz<br>Line rate (Gb/s) 6.6<br>Link rate (Gb/s) 6.6<br>EXOSTIV dock output  | A 132 MHz reference clock is generated with the<br>EXOSTIV Probe.<br>With this reference clock, we are able to configure<br>the GTH at 6.6 Gbps   |
| Int<br>Int<br>Int<br>Int<br>Vive | fo :<br>fo : License is activated, expiration : 2020-01-01 00:00:00<br>fo :<br>fo : Project file "C:/Projects/Cisco/KCU105-1SFP-link.epf" loa<br>ado link X [ EXOSTIV Probe X [ FPGA link X | Log Window  |



#### 'KCU105-2SFP-link.epf' :

This configuration is essentially the same as the previous one, except that 2 SFP links are used for upstream data (MGT\_TxP1 of bank 226 at pin W4 is used). Hence, the total data rate is 13.2 Gbps.

| EXOSTIV Das<br><u>T</u> ools <u>H</u>   | hboard - C:/Projects/Cisco/KCU105-2SFP<br>elp  | inks.epf — 🗆                       | × |
|---|--|------------------------------------|---|
| Link<br>Configuratio  | Capture<br>Configuration   | Run Debug<br>Insertion Design      |   |
| FPGA Type   |  | Connector                          |   |
| Family  | Kintex UltraScale 🔻  | Connector type SFP                 |   |
| Package   | ffva1156 👻   |                                    |   |
| Speed grade   | -2 🔻   |                                    |   |
| Part  | xcku040-ffva1156-2-e 🔻   |                                    |   |
| Upstream Link   |  | Downstream Link                    |   |
| Transceiver b   | ank 226 🔻  | ◯ Use I2C link                     |   |
| MGT type  | GTH  | Transceiver bank 226               |   |
| MGT_TxP0  | AA4  | MGT_RxP0 Y2                        |   |
| MGT_TxP1  | W4   |                                    |   |
| MGT_TxP2  | U4   | MGT_RxP2 T2                        |   |
| MGT_TxP3  | R4   | MGT_RxP3 P2                        |   |
| Reference Clo<br>Transceiver b<br>MGT_REFCLK<br>MGT_REFCLK<br>Frequency (M<br>Line rate (Gb/<br>Link rate (Gb/<br>EXOSTIV dod | dk<br>ank 226 ▼<br>P0 V6 ✓<br>P1 T6 □<br>Hz) 132 @<br>Range : 60 MHz to 280 MHz<br>s) 6.6 ▼<br>s) 13.2 :<br>:output ✓  |                                    |   |
|   |  | .og Window                         |   |
| : License is ac<br>:<br>: Project file "<br>: Project file "  | tivated, expiration : 2020-01-01 00:00:00<br>C:/Projects/Cisco/KCU 105-1SFP-link.epf <sup>®</sup> load<br>C:/Projects/Cisco/KCU 105-2SFP-links.epf <sup>®</sup> load | l successfully.<br>d successfully. |   |

#### What if you prefer to use a reference clock from the KCU105?

It is possible to use an alternative clock source for the transceivers connected to the SFP+ of KCU105. The source clock can come from the same bank (226) or – from adjacent banks 225 or 227 (see clock source bank selection below).

| MG1_TXP2       | U4  |                           | $\leq$  | MGT RxP2 |
|----------------|-----|---------------------------|---------|----------|
| MGT_TxP3       | R4  |                           |         | MGT_RxP3 |
| Reference Cloc | :k  |                           |         |          |
| Transceiver ba | ank | 226                       | •       |          |
| MGT REFCLK     | P0  | 225                       |         |          |
|                | 0   | 226                       |         |          |
|                |     | 227                       |         |          |
| Frequency (M   | HZ) | 132                       | w later |          |
|                |     | Range : 60 MHz to 820 MHz |         |          |
| Line rate (Ch/ |     | 6.6                       |         |          |



The following clock sources could be used:

**Quad 225 :** the only clock connected here is the PCIe clock of the edge connector. Can be an option if it is connected to a valid low jitter clock.

**Quad 226:** MGT\_REFCLK\_P1/N1 – (P is on pin T6), connected to FMC\_LPC\_GBTCLKO\_M2C\_C\_P/N – that is one of the clocks on the FMC **low pin count** (LPC) connector. Can be an option if there is a proper mezzanine card plugged in the FMC LPC connector, with the adequate source oscillator.

Quad 227: MGTREFCLK0 - MGT\_SI570\_CLOCK\_C\_P/N clock or MGTREFCLK1 - SI5328\_OUT\_C\_P/N jitter attenuator clock : these 2 on-board clock generators can be used as a reference. Care must be taken to properly program them to the desired frequency and enter it in the 'Frequency (MHz)' field in the link configuration page. This is probably the best alternative option, but requires the proper initialization to a known frequency.

# Using EXOSTIV with KCU105 evaluation kit through FMC HPC

In this section, we show how to use the KCU105 evaluation kit with the FMC HPC connector. As described below, connecting the EXOSTIV Probe to the KCU105 through the FMC HPC connector requires using an adapter. In this example, we'll use the FMC to HDMI adapter (ref <u>EA-HDMI-FMC-01 – click on this link</u>).

#### **KCU105** : overview





#### **Reviewing the .epf file settings**

The provided configuration file KCU105-HDMI-4links-HPC-1.epf supposes using the <u>FMC to HDMI module adapter</u> ref EA-HDMI-FMC-01 for connectivity between the FMC HPC connector of the KCU105 board and the EXOSTIV Probe, through its HDMI connector.

If another adapter is used (FMC to HDMI or FMC to SFP/SFP+), the configuration described below must be adapted accordingly.

**Remark:** the FMC HPC connector of the KCU105 provides alternate possibilities for transceiver choice and clocking. They are summarized in Table 1.

| EXOS  | TIV Dasł<br>ols He  | hboard for Xilinx   | - D:/Projects/ | Xplorer/Pro  | oduct/Support/Xilinx                     | EvalKits/KCU1   | 05/KCU105-Ref-EPF-1  | - 0  | ×      |
|---|---|---|----------------|--------------|--|---|--|--|--------|
|   | The FMC HPC connector of the KCU105 board is<br>connected to 8 transceivers. In this example, we<br>select 4 transceivers from hank 228 |   |                |              |  |   |  |  |        |
| Cor   | Link<br>nfiguratio  | in <b>2</b> 2   | 2 Cr           | onfiguration | 222                                      | EXOSTIV   | /IP >>>  | Debug<br>Design  |        |
| FPGA  | Туре  |   |                |              | Connector                                |   |  |  |        |
| Family                                      | ł   | Kintex UltraScale   | /              | -            | Connector type                           | HDMI  | • •  |  |        |
| Packa                                       | ge f  | ffva1156  | /              | -            |  |   | We use the 'HDMI'  | connector tw   |        |
| Speed                                       | l grade   | -2  | /              | -            |  |   | the probe (the HD  | MI connectiv   | ity is |
| Part  | 2   | kcku040-ffva1156  | 5-2-е          | •            |  |   | provided by the FM   | C adapter we   | use).  |
| Upstre                                      | eam Link  |   |                |              | Downstream Link                          |   |  |  |        |
| Transo                                      | ceiver ba   | nk 228  | •/             | -            | 🖲 Use I2C link                           | O Use transc  | eiver link   | - i  |        |
| MGT t                                       | ype   | GTH /   | /              |              | SCL package pin                          | H11   | ~  | - i  |        |
| MGT_  | TxP0  | F6 🕨  |                |              | SDA package pin                          | G11   | ~  | 1 - C  |        |
| MGT_  | TxP1  | D6  |                |              | SCL I/O standard                         | LVCMOS18  | •  |  |        |
| MGT_  | TxP2  | C4  |                |              | SDA I/O standar                          | LVCMOS18  | <b>•</b>   | 1 - C  |        |
| MGT_  | TxP3  | B6  |                |              | I/O voltages bel                         | w 2.5V require:   | s an external  |  |        |
| Refere<br>Transo<br>MGT_1<br>MGT_1<br>Frequ | ence Cloc<br>ceiver ba<br>REFCLK_<br>REFCLK_<br>ency (MH  | k<br>nk <u>228</u><br>P0 <u>K6</u><br>P1 <u>H6</u><br>iz) 125 |                |              | H11 a<br>pins o<br>HDM<br>guide<br>selec | and G11 are<br>of the FMC co<br>adapter spe<br>, VADJ is se<br>ed for both. | the 'LAOO_P_CC' and '<br>onnector, as specified in<br>c. As specified in the KC<br>t to 1.8V – hence 'LV | LA00_N_CC'<br>the FMC to<br>CU105 user's<br>CMOS18' is |        |
| Line ra                                     | ate (Gb/s   | Range : 6   | 0 MHz to 650 M | Hz           | We chose                                 | one of the 2  | clocking possibilities fro   | om bank  | Ţ      |
| Link ra                                     | ate (Gb/s   | ) 25  |                |              | 228. Thes                                | e 2 reference   | clocks for the transceiv   | vers are   |        |
| PLL ty                                      | pe used   | CPLL  |                |              | the clock                                | will be provi   | ided by the FMC adapt  | ter. We  |        |
| EXOST                                       | TIV clock   | output 🔄  |                |              | choose 12<br>to select a                 | 5 MHz as ref<br>6.25 Gbps d   | erence clock, which ena<br>ata rate on each transc   | ables us<br>eiver.                                     |        |
|   |   |   |                |              | <br>Log Window                           |   |  |  |        |
| guing                                       |   |   |                |              | Log Window                               | 1   |  |  |        |
| ۲<br>۲                                      |   |   |                |              |  |   |  |  |        |
| Console                                     |   |   |                |              |  |   |  |  |        |
| Netlist flow                                | Vivado  | ink 💢 🛛 EXOS  | TIV Probe X    | FPGA link    | *  |   |  |  |        |



:

| Table 1: FMC HPC to HDMI settings |  |
|-----------------------------------|--|

| Setting         | Value  | Comment  | Alternate possibilities   |
|-----------------|--|--|---|
| Connector type  | HDMI   | In this example, we use a FMC to HDMI<br>adapter. Hence, the connectivity to the<br>EXOSTIV Probe will be HDMI.  | With a FMC to SFP or QSFP<br>would make it possible to use<br>the 'SFP' connector(s) of the<br>EXOSTIV Probe.   |
| Upstream link   | Transceiver bank 228<br>MGT_TXP0 : F6<br>MGT_TXP1 : D6<br>MGT_TXP2 : C6<br>MGT_TXP3 : B6 | The FMC HPC connector on the KCU105 board<br>(connector J22) is connected to 8 transceivers<br>: 4 from bank 228 (as used here) and 4 from<br>bank 227   | Use the bank 227 transceivers:<br>MGT_TXP0 : N4<br>MGT_TXP1 : L4<br>MGT_TXP2 : J4<br>MGT_TXP3 : G4<br>When using this alternate<br>bank, the options for the<br>reference clock source are<br>different, as the source clock<br>can come from bank 227 or an<br>adjacent bank (226 or 228).<br>Check the board pinout in the<br>KCU105 user's guide to identify<br>the proper clock source. |
| Reference clock | Transceiver bank 228<br>MGT_REFCLK_P0 (K6)   | We use the clock reference mapped onto the<br>FMC connector. This clock has to be supplied<br>– we use the EA-FMC-HDMI-01 (FMC to HDMI<br>adapter) reference clock oscillator.<br>We choose 125 MHz as a value for the<br>frequency of this clock. The dip switches<br>settings on the FMC adapter must be set to<br>this value. | Use MGT_REFCLK_P1 (H6), also<br>supplied from the FMC<br>adapter.<br>Use an adjacent bank clock<br>(bank 227) – pins P6 or M6,<br>connected to SI570 or SI5328<br>clock oscillators on the board.<br>Check the value of the<br>frequencies of the clocks<br>generated with these on-board<br>components.  |
| Downstream link | Use I2C link<br>SCL Package: H11<br>SDA package: G11<br>SCL, SDA std:<br>LVCMOS18        | Using the EA-FMC-HDMI-01 adapter, the I2C<br>bus is made available from pins LA00_P_CC<br>and L00_N_CC of the FMC connector (please<br>check the FMC adapter user's guide).<br>These pins are connected to the FPGA H11<br>and G11.  | If another FMC to HDMI<br>adapter is used, check on<br>which pins the I2C adapter is<br>mapped.<br>If an adapter goes from FMC to<br>SFP/QSFP, then the probe<br>connector type is set to SFP<br>and one of the transceivers is<br>used for the downstream link.  |



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