

EXOSTIV

Using the VCU108 Virtex Ultrascale evaluation kit

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References

Revision History

Revision	Modifications
1.0.0	<ul style="list-style-type: none">Initial revision

EXOSTIV – using the VCU108 kit

Introduction

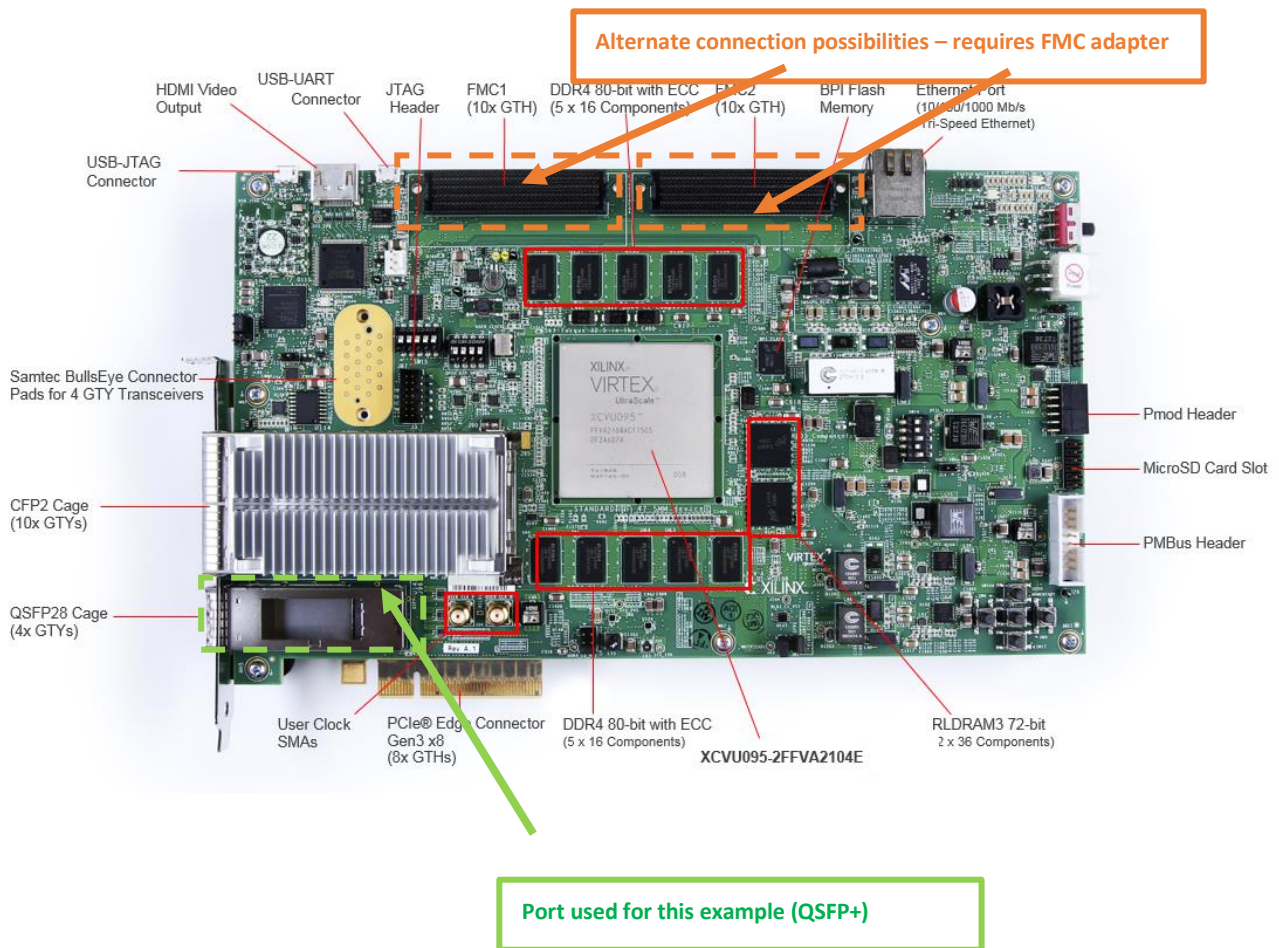
This document provides information about using EXOSTIV with the VCU108 Virtex Ultrascale evaluation kit (<https://www.xilinx.com/products/boards-and-kits/ek-u1-vcu108-g.html>).

Using EXOSTIV with the VCU108 evaluation kit

EXOSTIV can be connected to the VCU108 evaluation kit through the QSFP+ connector with a QSFP+ to 4x SFP+ cable with splitter or through another connector (e.g. the FMC HPC), possibly with an adapter.

In this document, we'll describe how to use EXOSTIV with the VCU108 QSFP+ connector. We provide a .epf file to be used with the EXOSTIV Dashboard, that is pre-configured for use with this port.

VCU108 : overview



Connecting the VCU108



All the 4 transceivers of EXOSTIV Probe are connected with a 4xSFP+ to QSFP+ cable.

Reviewing the .epf files settings for the link configuration

Using the SFP connectors on EXOSTIV Probe and the QSP+ port on the VCU108 board.

'demo-VCU108-1.8.2.epf' (for use with EXOSTIV Dashboard version 1.8.x)

The screenshot shows the EXOSTIV Dashboard for Xilinx configuration window. The main configuration area is divided into several sections:

- FPGA Type:** Family: Virtex UltraScale, Package: ffva2104, Speed grade: -2, Part: xcvu095-ffva2104-2-e.
- Connector:** Connector type: SFP.
- Upstream Link:** Transceiver bank: 127, MGT type: GTY, MGT_TxP0: AK42, MGT_TxP1: AJ40, MGT_TxP2: AG40, MGT_TxP3: AE40.
- Downstream Link:** Use I2C link: , Use transceiver link: . Transceiver bank: 127, MGT_RxP0: AG45, MGT_RxP1: AF43, MGT_RxP2: AE45, MGT_RxP3: AD43.
- Reference Clock:** Transceiver bank: 127, MGT_REFCLK_P0: AF38, MGT_REFCLK_P1: AD38, Frequency (MHz): 312.5, Line rate (Gb/s): 10.3125, Link rate (Gb/s): 41.25, PLL type used: QPLL, EXOSTIV clock output: .

Callouts provide additional context:

- Virtex UltraScale part mounted on the VCU108 board:** Points to the FPGA Type section.
- We use the SFP connector type on the EXOSTIV Probe:** Points to the Connector type dropdown.
- We select the 4 transceivers connected to bank 127 of the FPGA (refer to the VCU108 documentation to check this configuration). These are connected to the QSP+ port.** Points to the MGT_TxP and MGT_RxP checkboxes.
- When using the SFP connectors of EXOSTIV Probe, the downstream channel required for the IP is implemented by using one of the transceivers in full-duplex mode. We herewith select transceiver 0 of the bank used upstream (127)** Points to the MGT_RxP0 checkbox.
- In the provided example, we program the VCU108 board oscillator connected to bank 127 at pin AD38 automatically. The oscillator frequency is set to 312.5 MHz on the board. We match this setting here, so the IP can make use of this clock to generate traffic on the transceivers. From this frequency, we select a 'line rate' of 10.3125 Gbps per link. Hence, the total bandwidth on the transceivers is 41.25 Gbps.** Points to the Reference Clock section.

The console at the bottom shows the following messages:

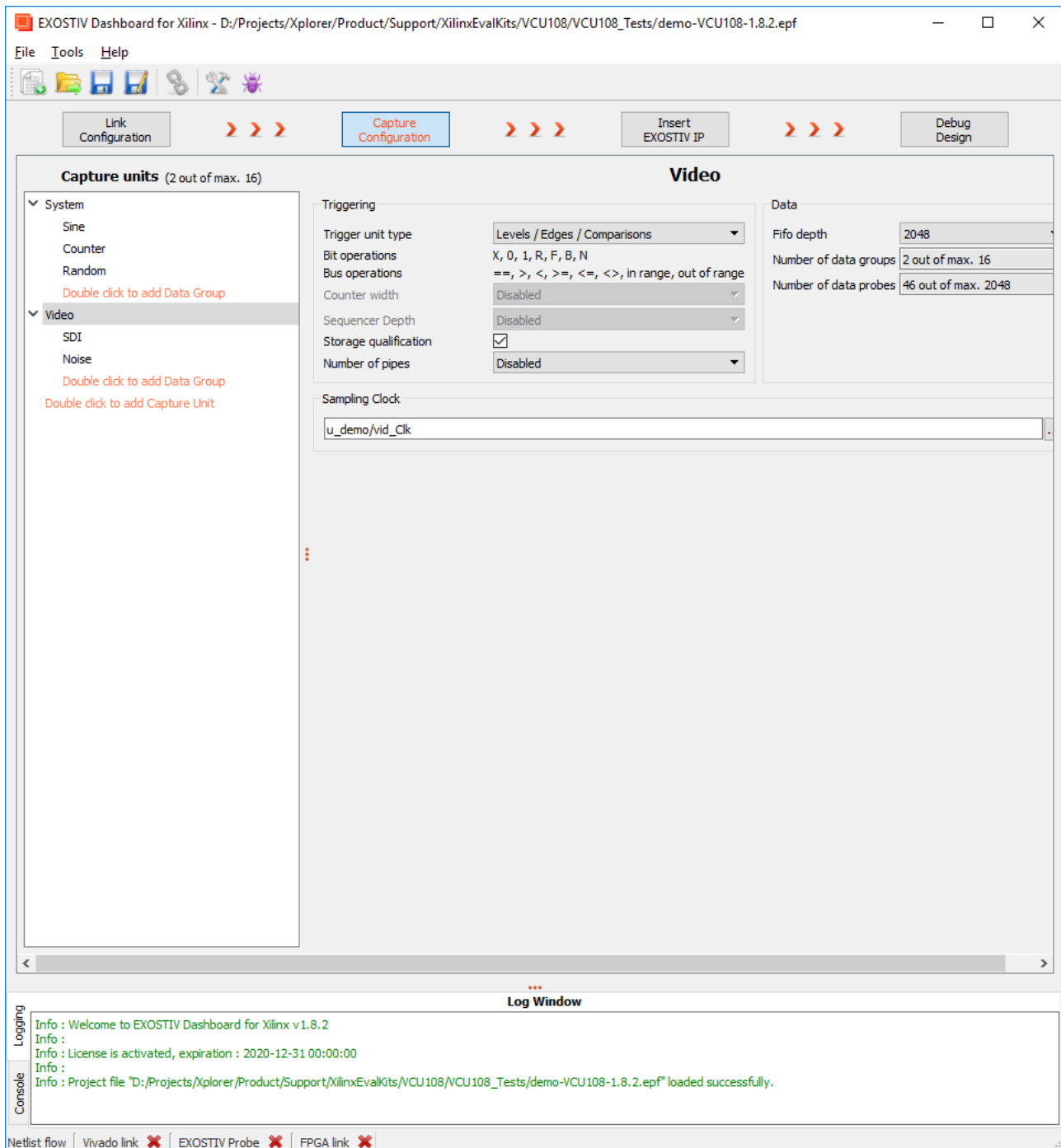
```

Info : Welcome to EXOSTIV Dashboard for Xilinx v1.8.2
Info :
Info : License is activated, expiration : 2020-12-31 00:00:00
Info :
Info : Project file 'D:/Projects/Xplorer/Product/Support/XilinxE
  
```

Reviewing the .epf files settings for the capture configuration

Please open the .epf files and review them through the EXOSTIV Dashboard interface.
Here are the main characteristics of the example:

- There are 5 data generators in the example design. There are connected to 2 capture units:
 - o 'System' capture unit (16 bits) – memory buffer: 1,024 samples.
 - Digital sine wave: 'Sine' data group
 - A counter: "Counter' data group
 - A pseudo random number generator: 'Random' data group
 - o 'Video Capture Unit' (46 bits) – memory buffer: 2,048 samples – Storage qualification enabled
 - Video (SDI) stream : 'SDI' data group
 - A set of data used to generate a sine wave with noise : 'Noise'.



The screenshot shows the EXOSTIV Dashboard for Xilinx interface. The main window is titled "EXOSTIV Dashboard for Xilinx - D:/Projects/Xplorer/Product/Support/XilinxEvalKits/VCU108/VCU108_Tests/demo-VCU108-1.8.2.epf". The interface includes a menu bar (File, Tools, Help) and a toolbar with icons for file operations and debugging. Below the toolbar are buttons for "Link Configuration", "Capture Configuration", "Insert EXOSTIV IP", and "Debug Design".

The main configuration area is divided into two sections: "Capture units (2 out of max. 16)" and "Video".

Capture units (2 out of max. 16):

- System:** Sine, Counter, Random. Includes a "Double click to add Data Group" button.
- Video:** SDI, Noise. Includes "Double click to add Data Group" and "Double click to add Capture Unit" buttons.

Video Configuration:

- Triggering:**
 - Trigger unit type: Levels / Edges / Comparisons
 - Bit operations: X, 0, 1, R, F, B, N
 - Bus operations: ==, >, <, >=, <=, <>, in range, out of range
 - Counter width: Disabled
 - Sequencer Depth: Disabled
 - Storage qualification:
 - Number of pipes: Disabled
- Data:**
 - Fifo depth: 2048
 - Number of data groups: 2 out of max. 16
 - Number of data probes: 46 out of max. 2048
- Sampling Clock:** u_demo/vid_Clk

At the bottom, there is a "Log Window" showing the following messages:

```

Info : Welcome to EXOSTIV Dashboard for Xilinx v1.8.2
Info :
Info : License is activated, expiration : 2020-12-31 00:00:00
Info :
Info : Project file "D:/Projects/Xplorer/Product/Support/XilinxEvalKits/VCU108/VCU108_Tests/demo-VCU108-1.8.2.epf" loaded successfully.
  
```

The status bar at the bottom shows "Netlist flow", "Vivado link" (with a red X), "EXOSTIV Probe" (with a red X), and "FPGA link" (with a red X).

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