		TOTAL (device)	Used by EXOSTIV IP	EXOSTIV IP / FPGA
1 x CU x 2K nodes with 1k buffer - Reduced trigger logic (2K nodes total)				
Kintex Ultrascale	**CLB LUT**	242400	23481	**10%**
xcku040ffva1156-2	**CLB Registers**	484800	33593	**7%**
	Block RAM tiles	600	65	**11%**
Virtex Ultrascale 440 - Insertion of EXOSTIV IP - 4 x CU x 2,048 nodes + 1 x CU x 1,024 nodes (9k nodes total) with 1 k buffer each - Full trigger logic and storage qualification				
Virtex Ultrascale	**CLB LUT**	2532960	230341	**9%**
xcvu440flga2892-2	**CLB Registers**	5065920	238826	**5%**
	Block RAM tiles	2520	291	**12%**
Virtex Ultrascale 440 - Insertion of EXOSTIV IP - 16x CU x 2,048 nodes (32k nodes) with 1 k buffer each - Full trigger logic and storage qualification				
Virtex Ultrascale	**CLB LUT**	2532960	963146	**38%**
xcvu440flga2892-2	**CLB Registers**	5065920	826785	**16%**
	Block RAM tiles	2520	1032	**41%**
Virtex Ultrascale 440 - Insertion of EXOSTIV IP - 4x CU x 2,048 nodes (8k nodes) + 1 CU with 10x 2,048 (20k nodes) multiplexed - All CU buffers: 1,024 deep - Reduced trigger logic				
Virtex Ultrascale	**CLB LUT**	2532960	208933	**8%**
xcvu440flga2892-2	**CLB Registers**	5065920	261405	**5%**
	Block RAM tiles	2520	323	**13%**
Virtex Ultrascale 440 - Insertion of EXOSTIV IP - 2x CU x 2,048 nodes (4k nodes) with 2 k buffer each - Full trigger logic and storage qualification				
Virtex Ultrascale	**CLB LUT**	2532960	105571	**4%**
xcvu440flga2892-2	**CLB Registers**	5065920	106718	**2%**
	Block RAM tiles	2520	257	**10%**