Connection example between FPGA transceiver bank and ARF6-08 / ARF6-RA-08 connector

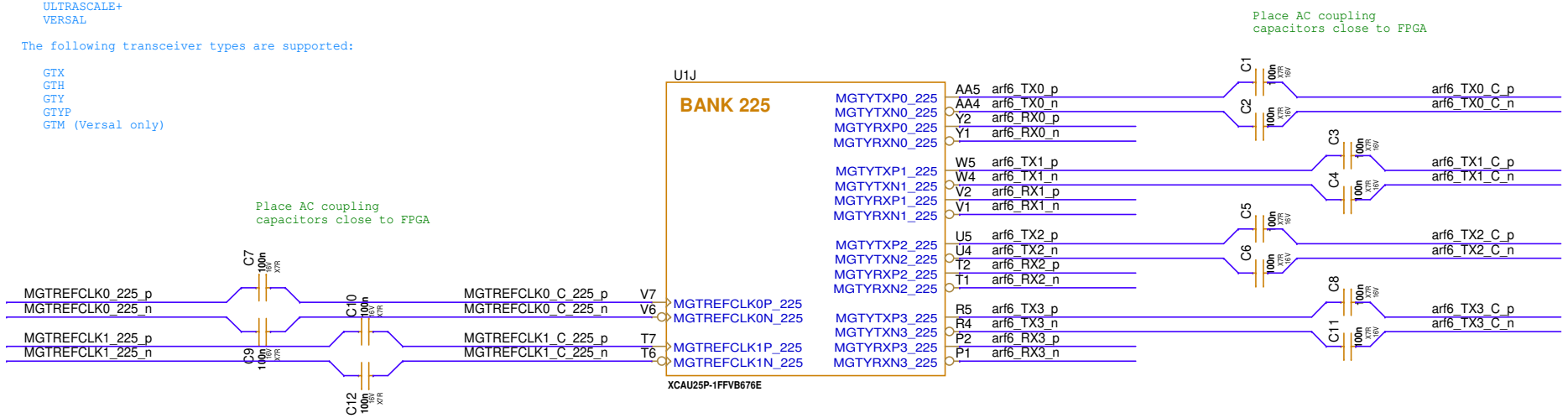
This example is based on Artix Ultrascale+ device.

Any device of the following families can be used:

- 7SERIE
- ULTRASCALE
- ULTRASCALE+
- VERSAL

The following transceiver types are supported:

- GTX
- GTH
- GTY
- GTYP
- GTM (Versal only)

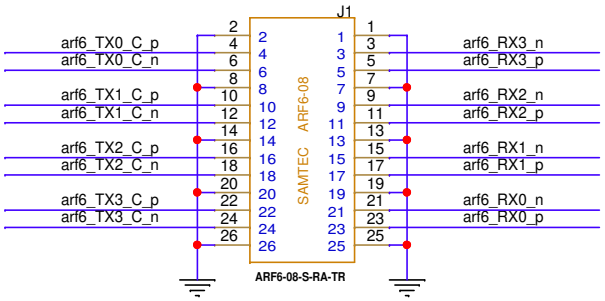


A reference clock must be provided to the transceiver bank
for proper operation. The clock can be applied locally to
REFCLK0 or REFCLK1 input port, or be internally routed from adjacent
transceiver banks.
(refer to AMD Xilinx device documentation for more details
and for applicable restrictions)

A single clock is required for the Exostiv IP.

Unused clock input port can generally be left floating/unconnected.
(refer to AMD Xilinx device documentation for more details)

Refer to the Exostiv Labs knowledge base to get the list
of recommeded clock frequencies.
https://www.exostivlabs.com/knowledgebase
Search for "reference clock frequencies"



The same pinout must be used for horizontal
or vertical connector.

SAMTEC part number:

vertical : ARF6-08-S-D-A-K-TR
horizontal: ARF6-08-S-RA-TR

IMPORTANT NOTES:

1. Pin swap within any TX or RX pair is allowed.
   This means that the P and N signals can be swapped within any pair.

2. The channel mapping between FPGA and connector can be changed,
   but the relative position of TX and RX pairs must be respected.
   This means that if a RX channel of the FPGA is connected
   to pair RX(i) on the connector (with i = 0,1,2 or 3),
   then the corresponding FPGA TX channel must be connected
   to pair TX(i) on the connector.

3. To use the Exostiv IP:
   - a single RX channel is required, more can be connected.
   - from minimum 1, to maximum 4 TX channels can be used.
   - all channels must come from the same QUAD.

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		Title: ARF6-08 — Size: A4
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Connection example between FPGA transceiver bank and QSFP28 connector for ACTIVE CABLE usage

This example is based on Artix Ultrascale+ device.

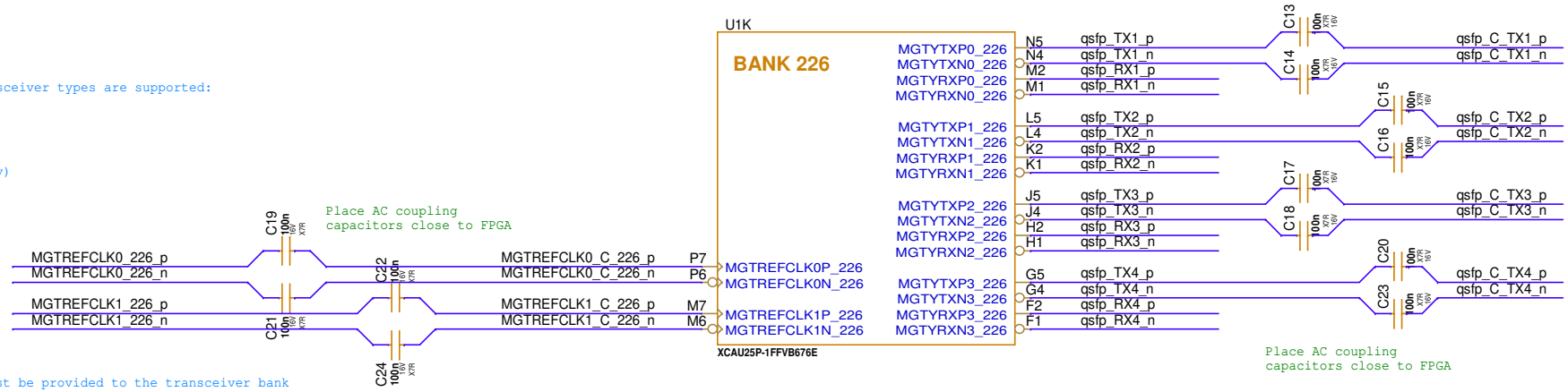
Any device of the following families can be used:

- 7SERIE
- ULTRASCALE
- ULTRASCALE+
- VERSAL

The following transceiver types are supported:

- GTX
- GTH
- GTY
- GTYP
- GTM (Versal only)

Transceiver Bank

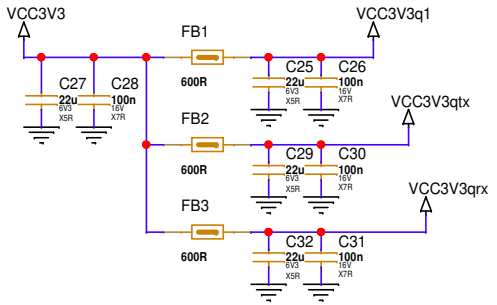


A reference clock must be provided to the transceiver bank for proper operation. The clock can be applied locally to REFCLK0 or REFCLK1 input port, or be internally routed from adjacent transceiver banks.
(refer to AMD Xilinx device documentation for more details and for applicable restrictions)

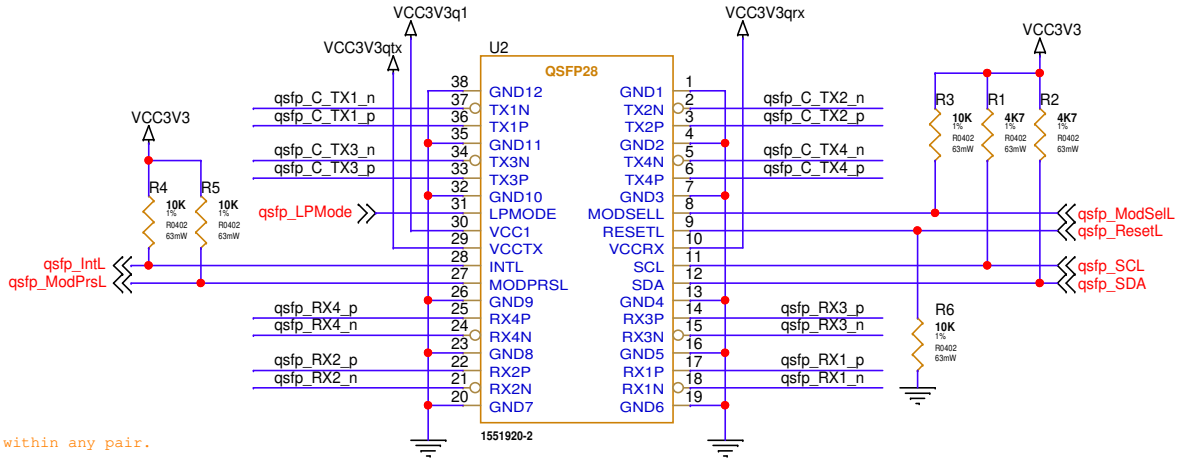
A single clock is required for the Exostiv IP.

Unused clock input port can generally be left floating/unconnected.
(refer to AMD Xilinx device documentation for more details)

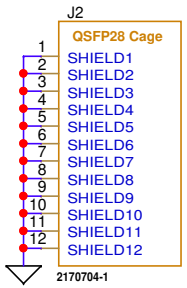
Refer to the Exostiv Labs knowledge base to get the list of recommeded clock frequencies.
https://www.exostivlabs.com/knowledgebase
Search for "reference clock frequencies"



QSFP28 Connector



QSFP28 Cage



IMPORTANT NOTES:

1. Pin swap within any TX or RX pair is allowed.
   This means that the P and N signals can be swapped within any pair.

2. The channel mapping between FPGA and connector can be changed,
   but the relative position of TX and RX pairs must be respected.
   This means that if a RX channel of the FPGA is connected
   to pair RX(i) on the connector (with i = 0,1,2 or 3),
   then the corresponding FPGA TX channel must be connected
   to pair TX(i) on the connector.

3. To use the Exostiv IP:
   - a single RX channel is required, more can be connected.
   - from minimum 1, to maximum 4 TX channels can be used.
   - all channels must come from the same QUAD.

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Variant: <Variant Name>

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Title	Size
QSFP28_ACTIVE	A4
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Connection example between FPGA transceiver bank and QSFP28 connector for PASSIVE CABLE usage

This example is based on Artix Ultrascale+ device.

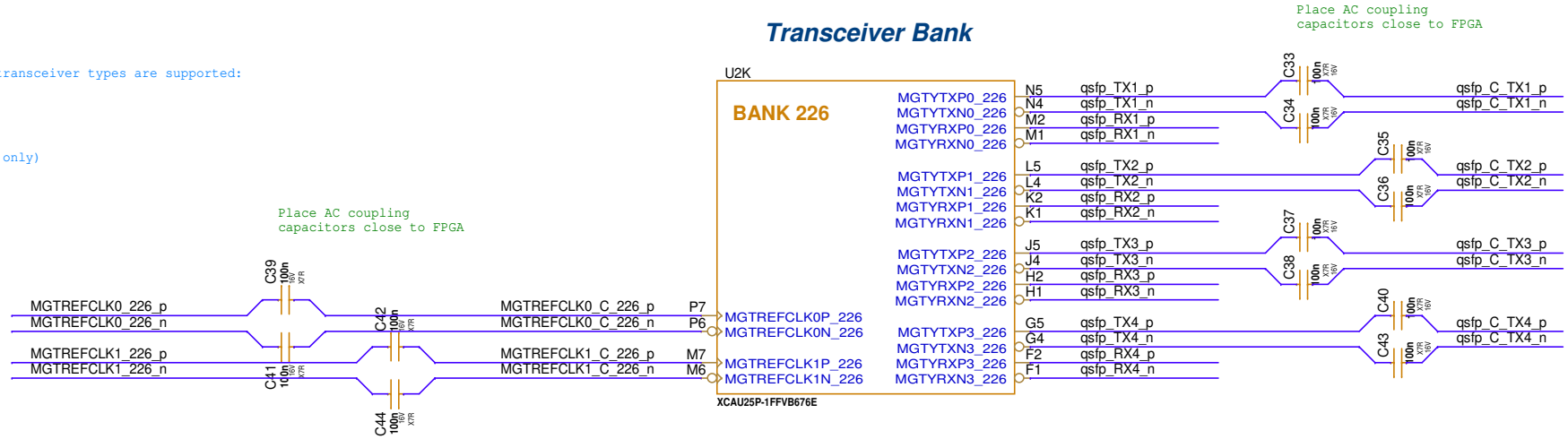
Any device of the following families can be used:

- 7SERIE
- ULTRASCALE
- ULTRASCALE+
- VERSAL

The following transceiver types are supported:

- GTX
- GTH
- GTY
- GTYP
- GTM (Versal only)

Transceiver Bank



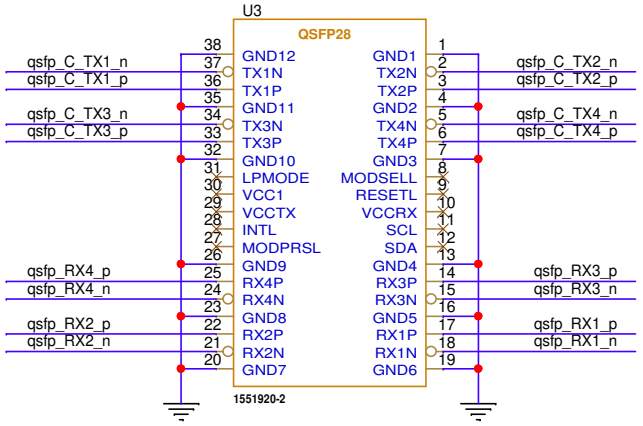
A reference clock must be provided to the transceiver bank for proper operation. The clock can be applied locally to REFCLK0 or REFCLK1 input port, or be internally routed from adjacent transceiver banks.
(refer to AMD Xilinx device documentation for more details and for applicable restrictions)

A single clock is required for the Exostiv IP.

Unused clock input port can generally be left floating/unconnected.
(refer to AMD Xilinx device documentation for more details)

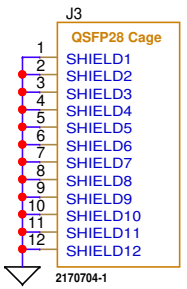
Refer to the Exostiv Labs knowledge base to get the list of recommeded clock frequencies.
https://www.exostivlabs.com/knowledgebase
Search for "reference clock frequencies"

QSFP28 Connector



If a passive QSFP28 cable is used, then all power and control pins of the QSFP connector can remain unconnected.
In this case, optical transceiver module can NOT be used.

QSFP28 Cage



IMPORTANT NOTES:

1. Pin swap within any TX or RX pair is allowed.
   This means that the P and N signals can be swapped within any pair.

2. The channel mapping between FPGA and connector can be changed, but the relative position of TX and RX pairs must be respected.
   This means that if a RX channel of the FPGA is connected to pair RX(i) on the connector (with i = 0,1,2 or 3), then the corresponding FPGA TX channel must be connected to pair TX(i) on the connector.

3. To use the Exostiv IP:
   - a single RX channel is required, more can be connected.
   - from minimum 1, to maximum 4 TX channels can be used.
   - all channels must come from the same QUAD.

EXOSTIV LABS

Variant: <Variant Name>

CONFIDENTIAL

Date: Wednesday, November 06, 2024

Title	Size
QSFP28_PASSIVE	A4
Project: CONN_EXAMPLE	Rev: 1.0
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