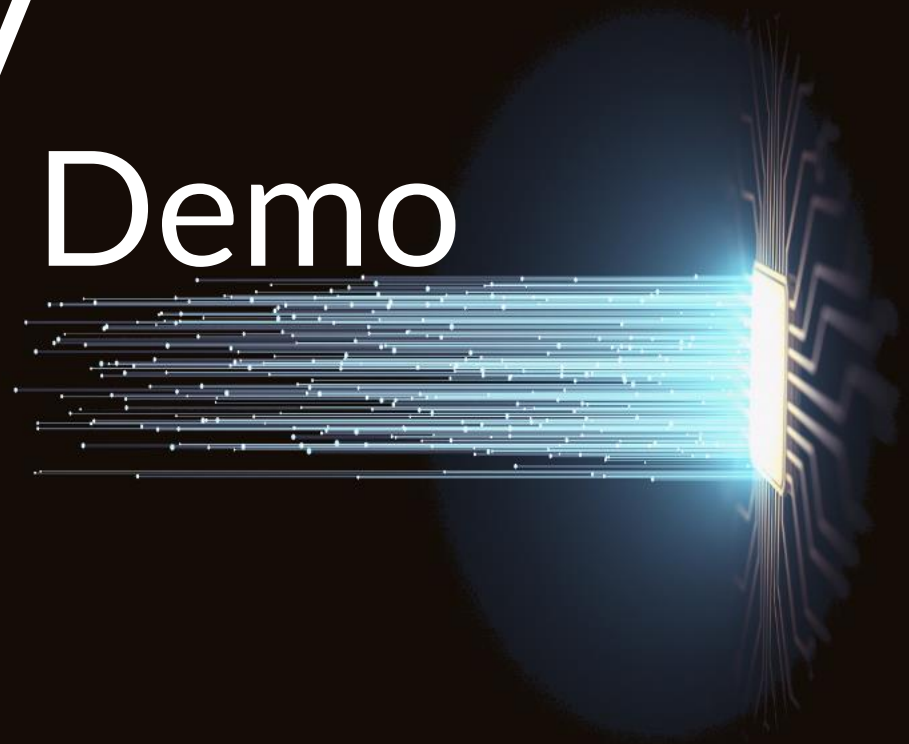
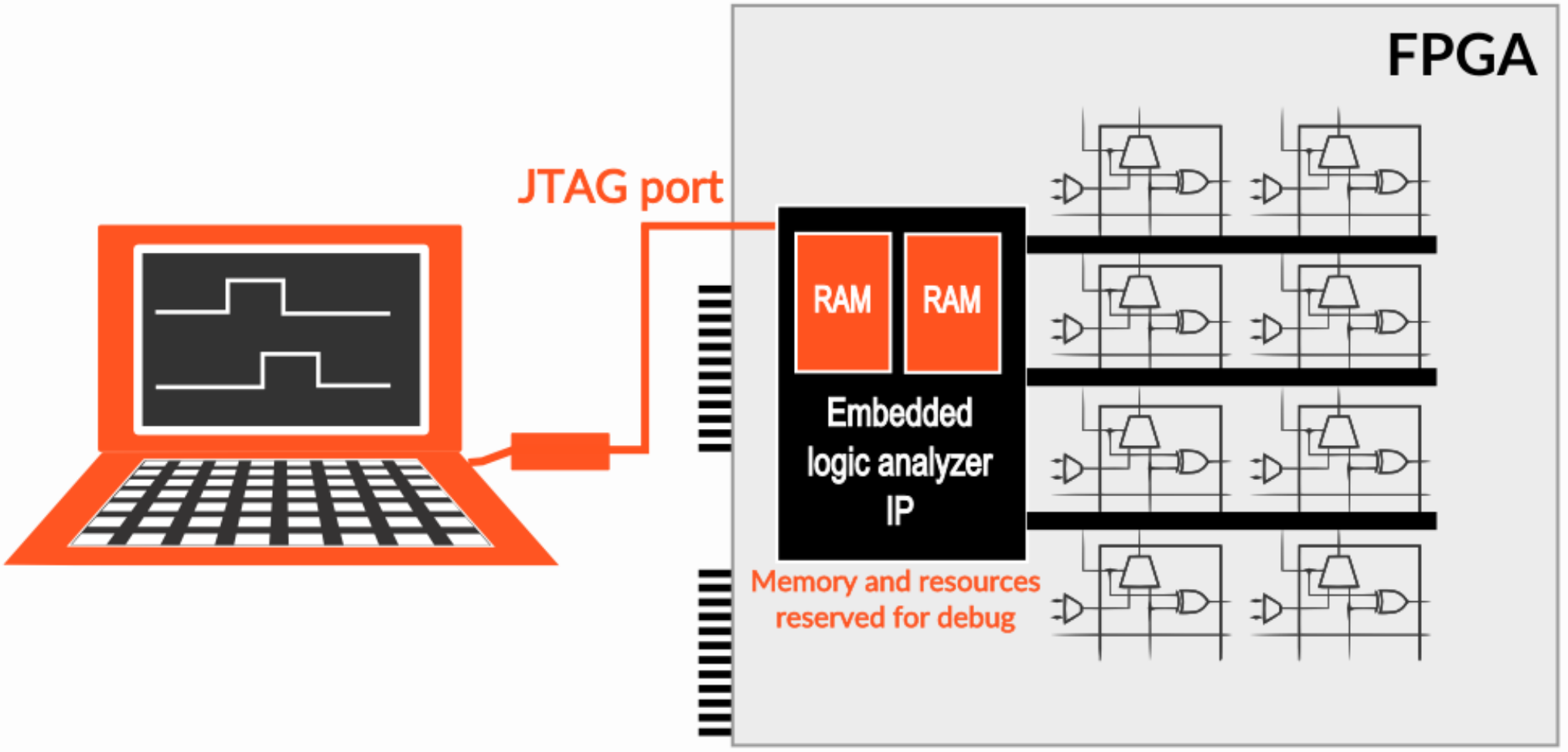
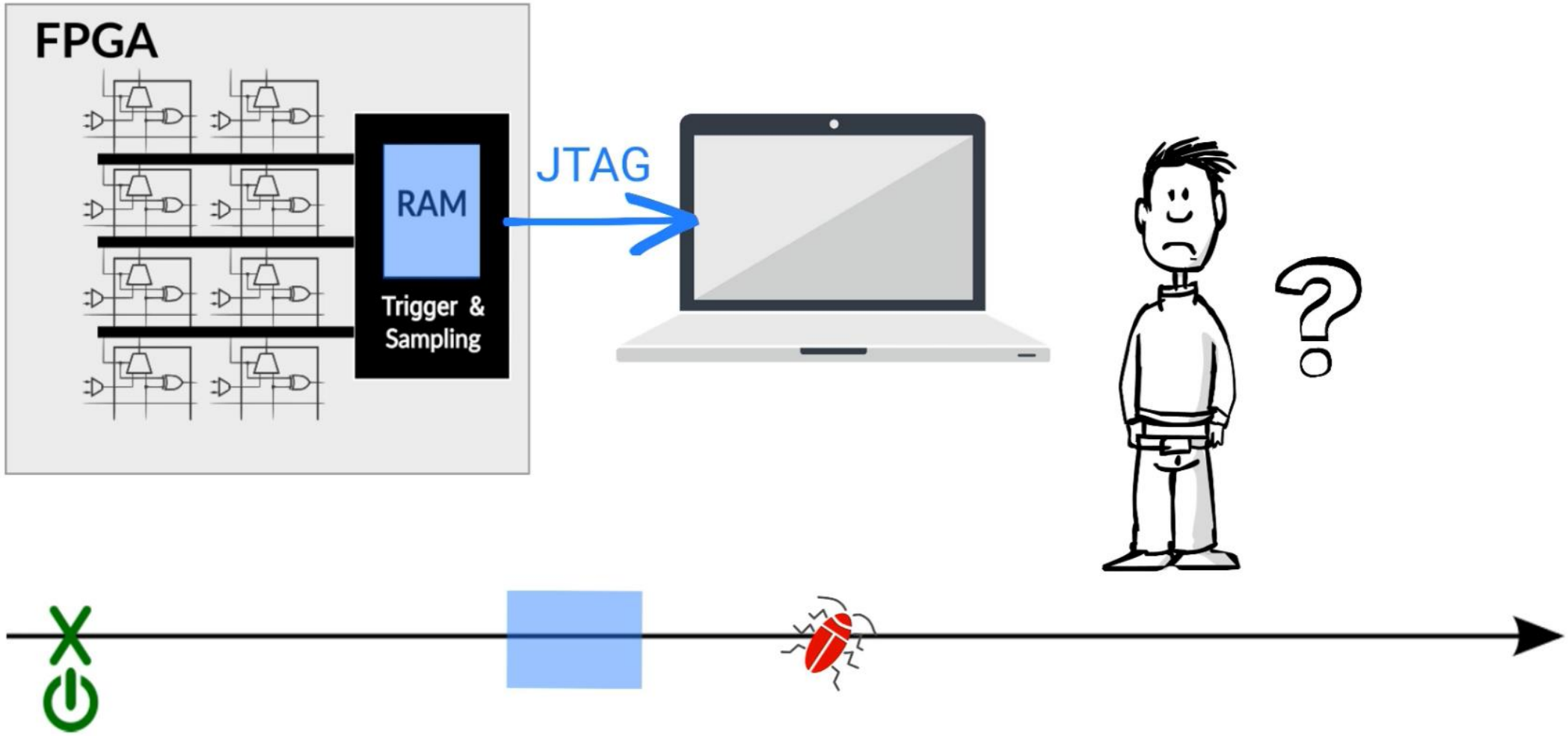
EXOSTIV LABS Visibility into the FPGA.

Exostiv
Presentation & Demo

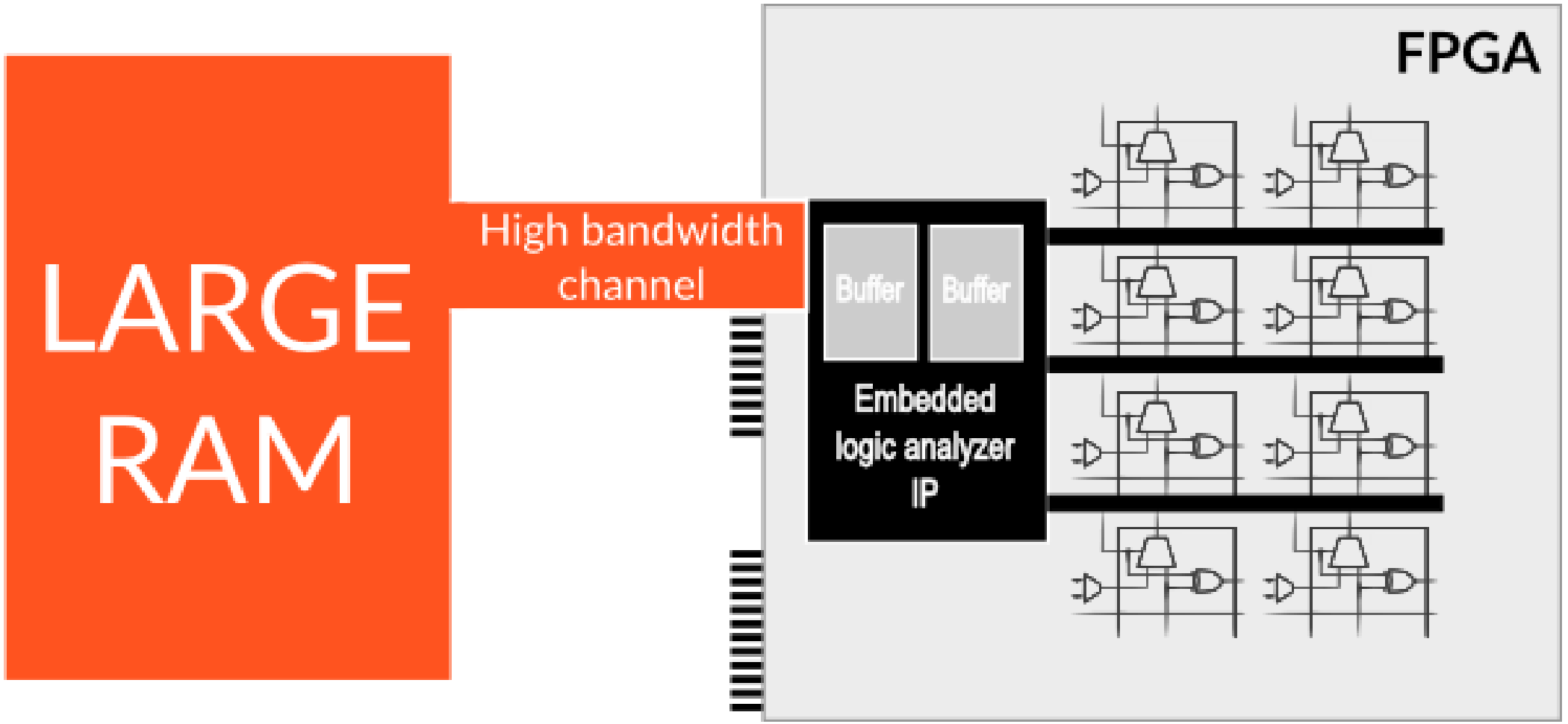


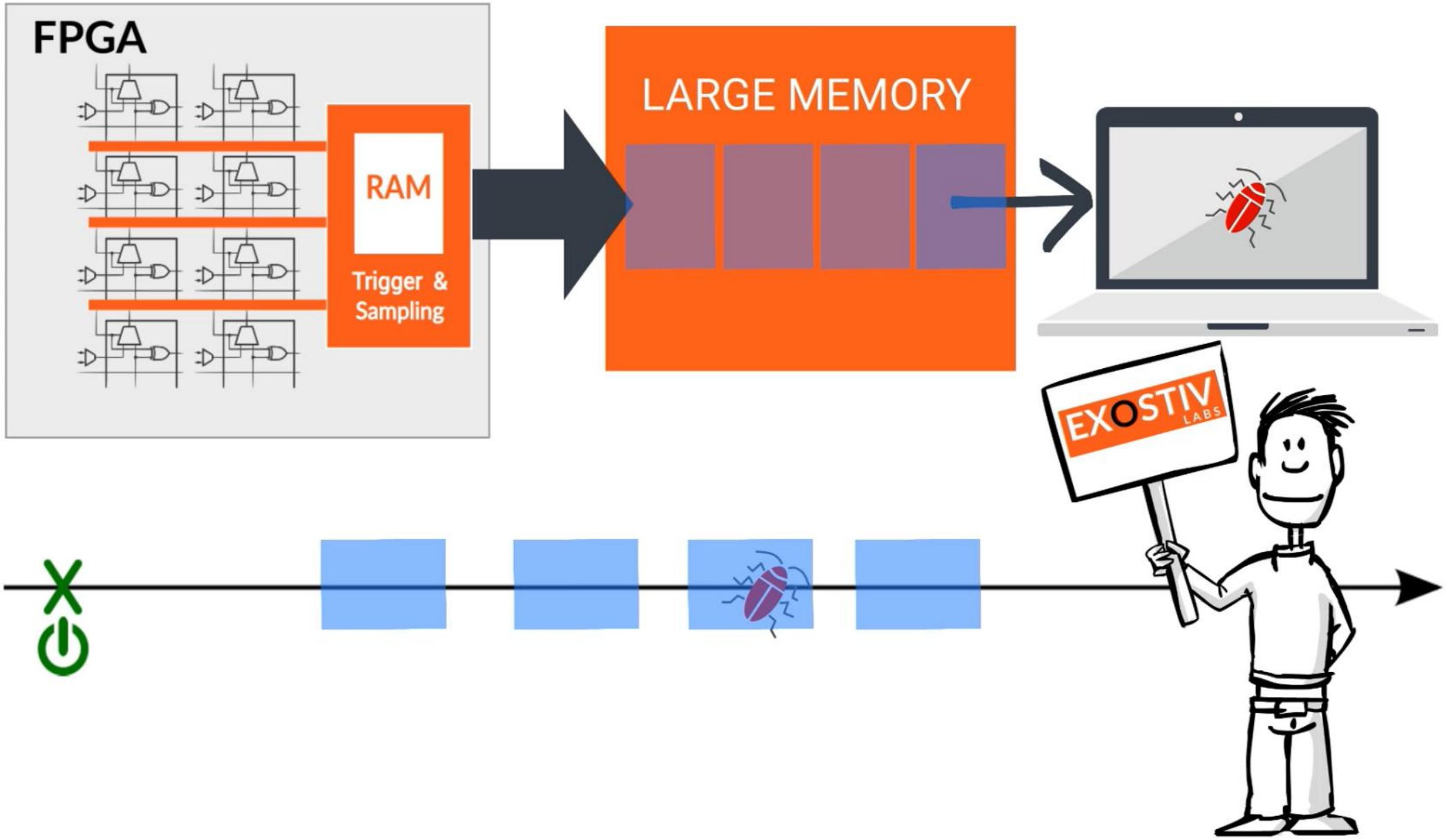
Debugging with a JTAG solution

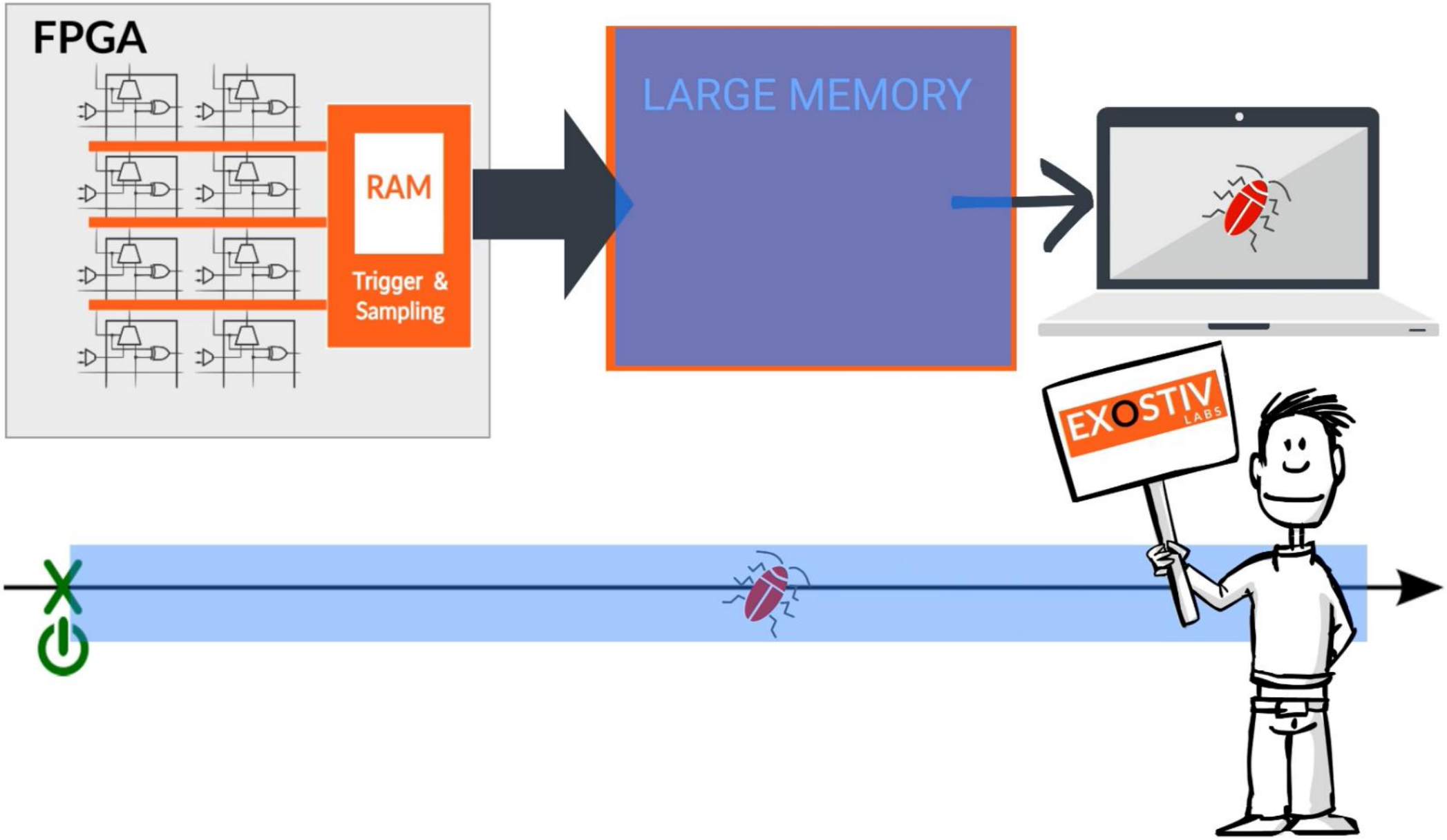



FPGA
RAM
Trigger &
Sampling
JTAG
?

EXOSTIV

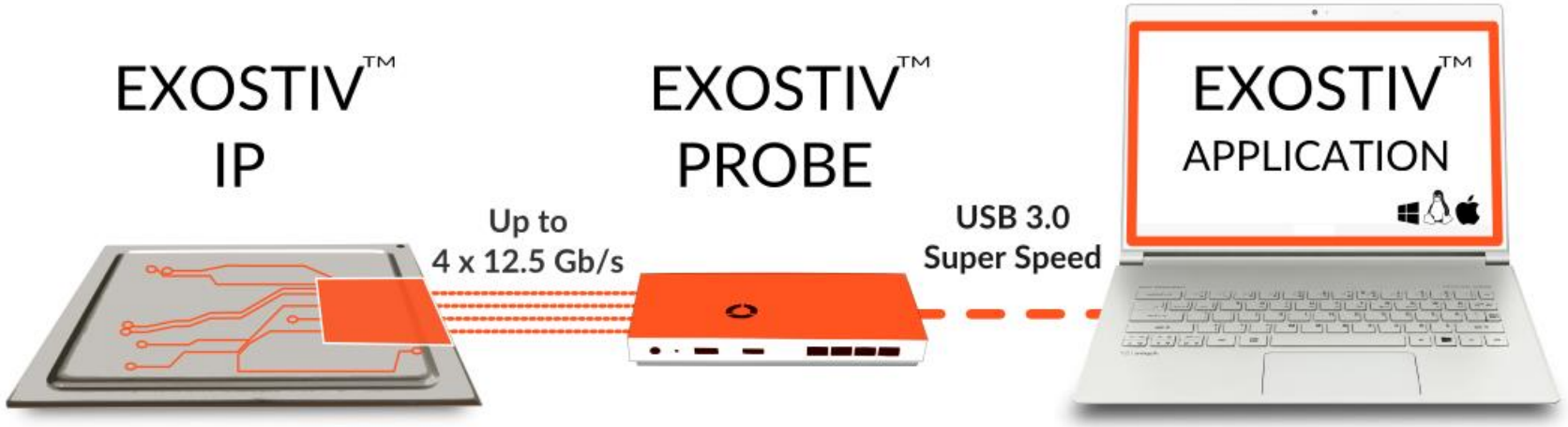

LARGE RAM
High bandwidth channel
FPGA
Buffer
Buffer
Embedded logic analyzer IP


FPGA
RAM
Trigger &
Sampling
LARGE MEMORY
EXOSTIV
LABS


FPGA
RAM
Trigger &
Sampling
LARGE MEMORY
EXOSTIV
LABS

EXOSTIV LABS Visibility into the FPGA.

EXOSTIV - Overview



Reach internal nodes

- Up to **16 capture units**
- Up to **16 data sets** per CU
- **1 trigger + 1 qualification unit** per CU
- Up to **2.048 nets** per data set
- IP RAM does not grow with capture size
- Sampling **@ system speed**

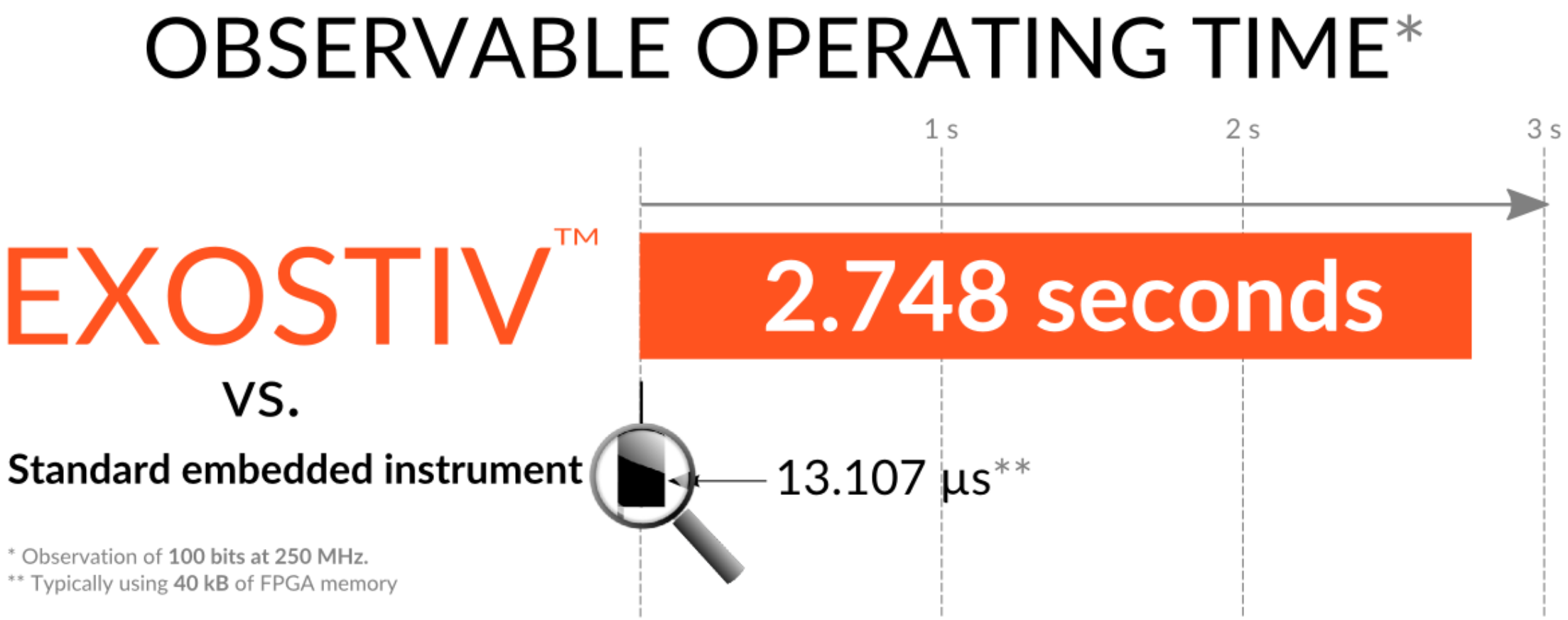
Extract trace

- Up to **8 GB** for trace storage
- Up to **4 x 12.5 Gbps** bandwidth
- Uses **Multi Gigabit Transceivers**
- **HDMI** and **SFP+** cage connector
- Optional connector adapters
- Downstream channel for IP control
- **USB 3.0** connection with workstation

Control & Analyze

- IP configuration & insertion
- Trigger and data filter set up
- IP communication and control
- Trace reception and encoding
- Advanced waveform viewer

Indicative gain



EXOSTIV Probe

High-speed connector – HDMI format – up to 4 x 10 Gbps

High-speed connectors – SFP+ format – up to 4 x 12.5 Gbps

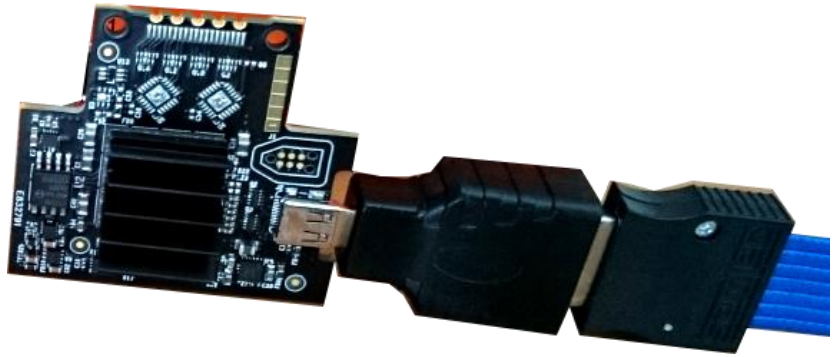
Connectivity

SFP+ or QSFP+
(copper / fiber)

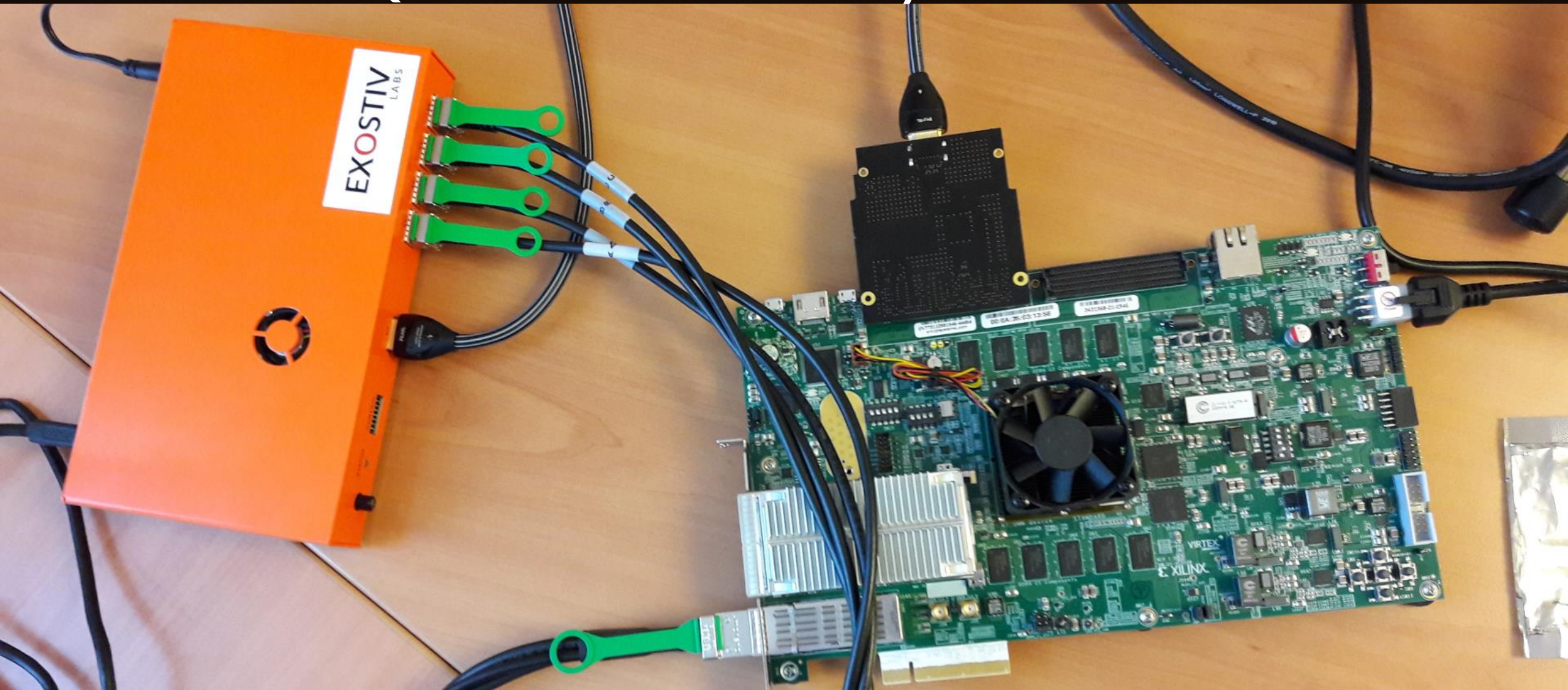
FMC HPC / LPC
(with adapter)

(New connectors under
qualification – Samtec, …)

Custom low footprint



FMC / QSFP connectivity



Custom low footprint connectivity

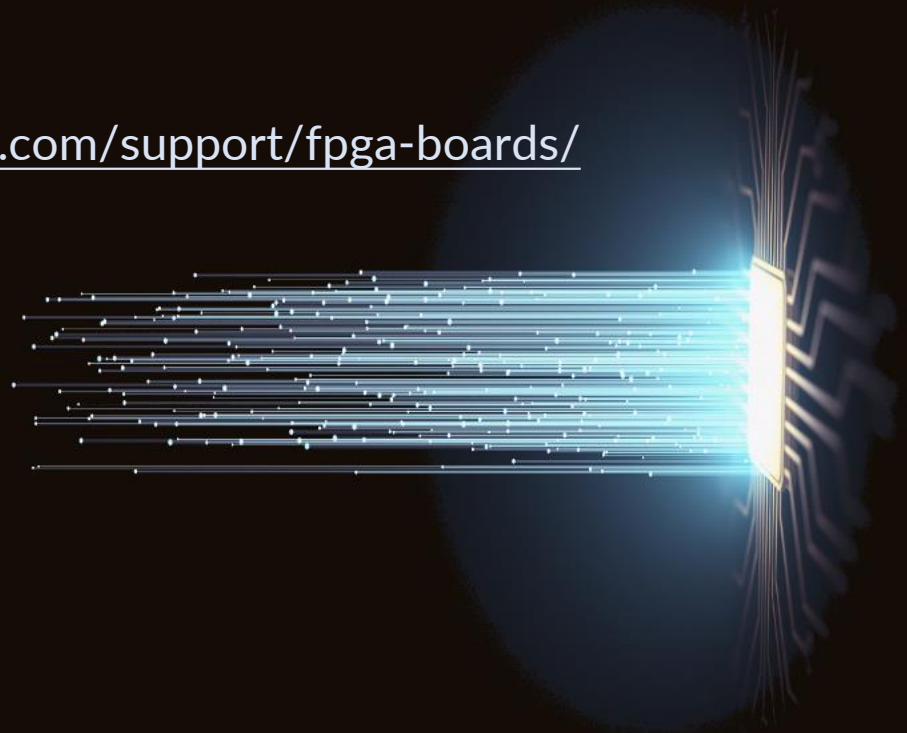
EXOSTIV LABS Visibility into the FPGA.

QSFP+ connectivity

Choose the board you like

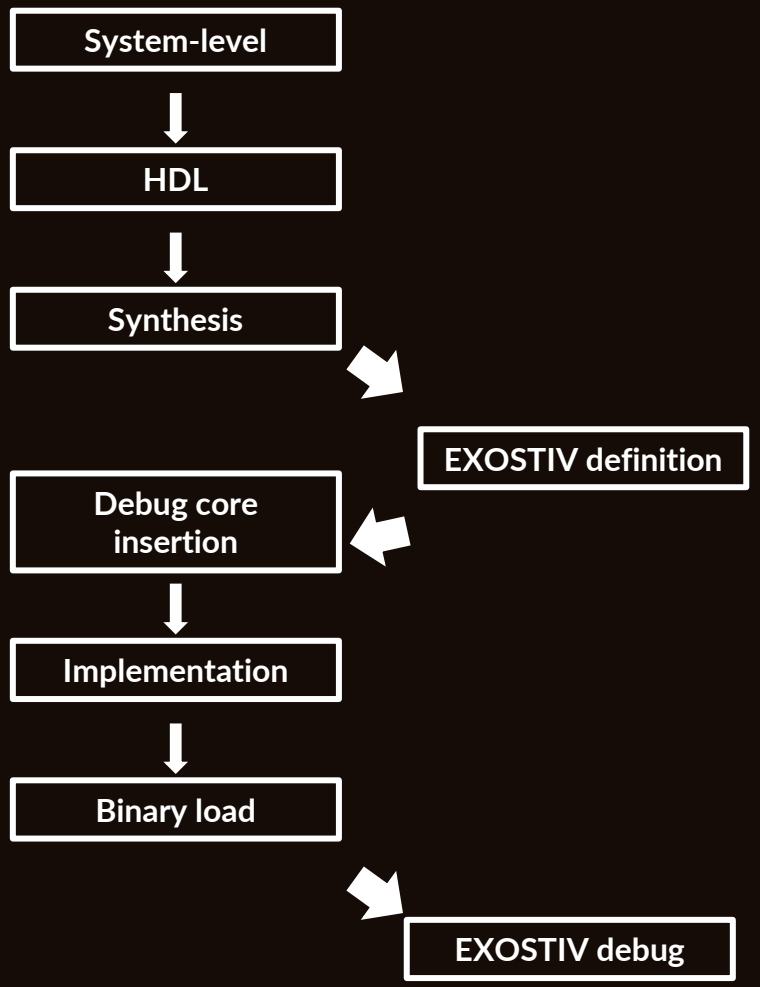
- Pick a standard FPGA board
  - Xilinx development kits
  - Intel development kits
  - The Dini Group / Synopsys
  - proFPGA
  - High Tech Global
  - Enclustra
  - REFLEX CES
  - …
- Use a FPGA board designed in-house
  - Add a custom connector
  - Use an existing connector, possibly with an adapter (See the Connecting Guide)

https://www.exostivlabs.com/support/fpga-boards/

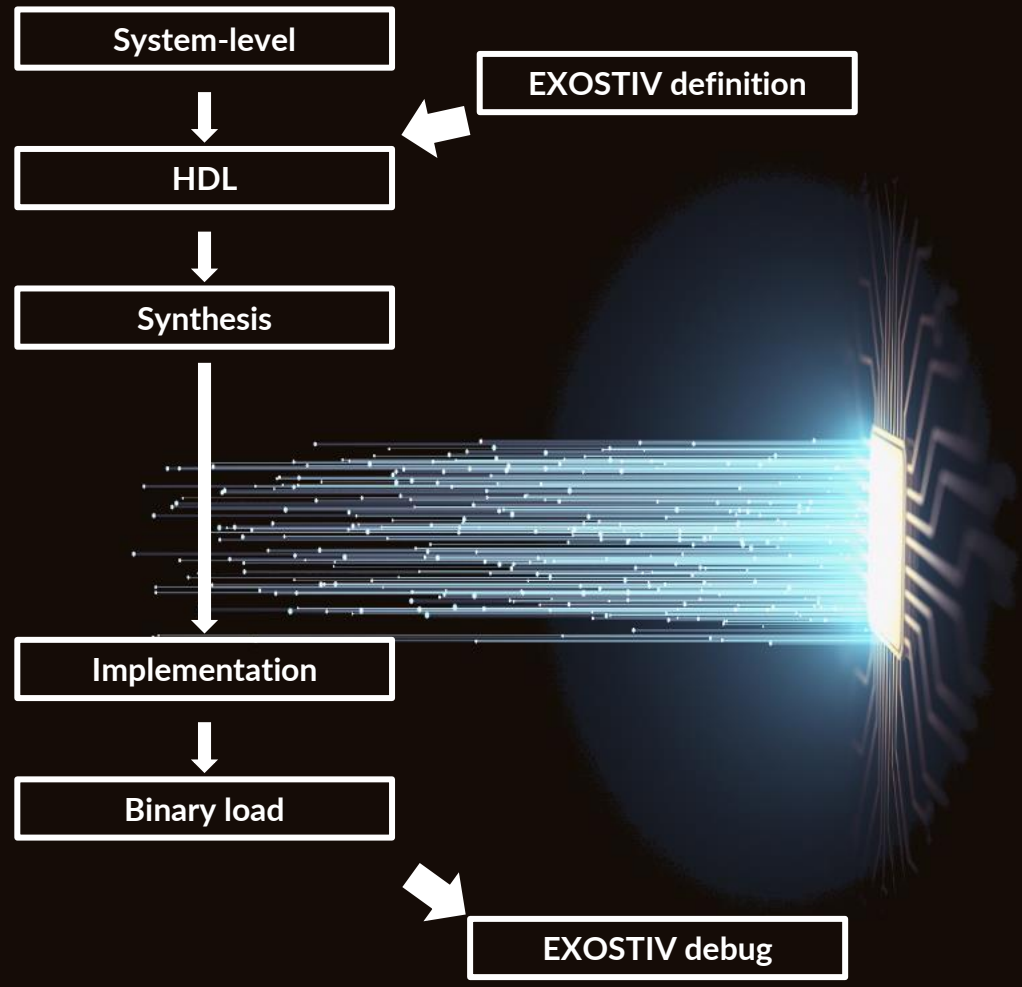


IP insertion flows

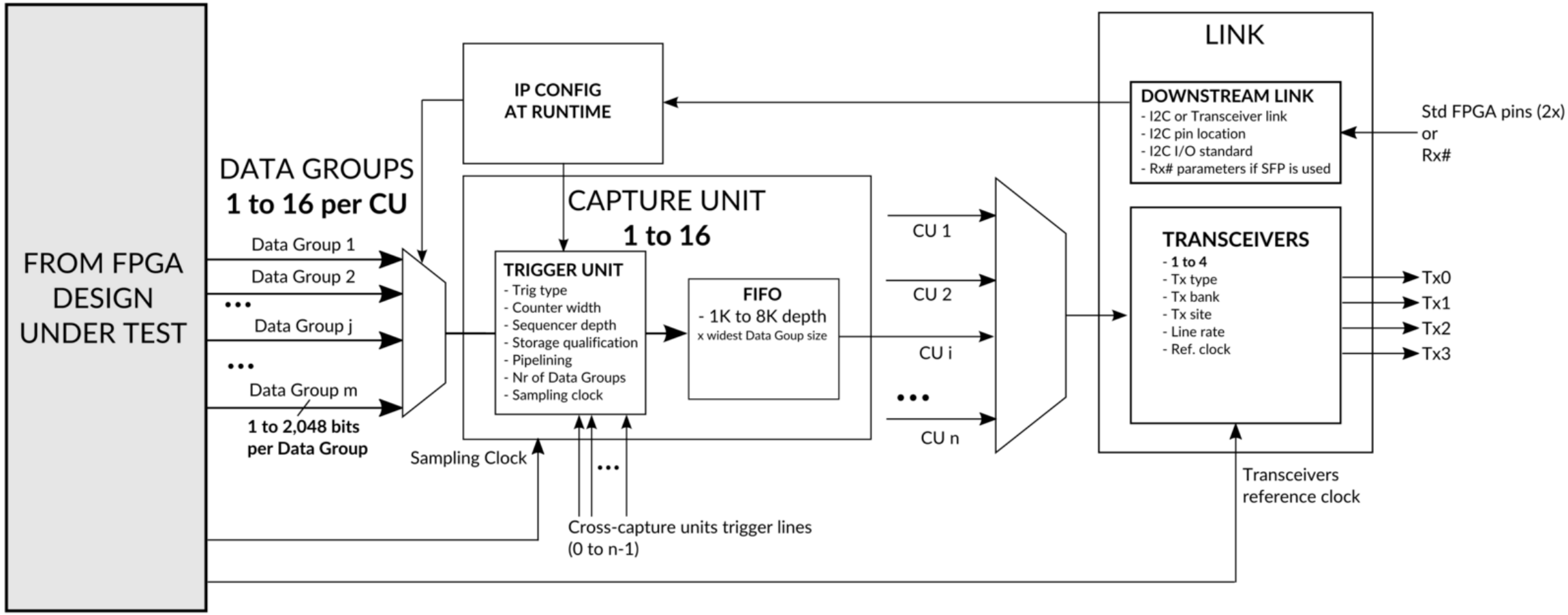
Netlist / Automatic flow



RTL / Manual flow



IP Overview


FROM FPGA DESIGN UNDER TEST
IP CONFIG AT RUNTIME
DATA GROUPS
1 to 16 per CU
Data Group 1
Data Group 2
Data Group j
Data Group m
1 to 2,048 bits per Data Group
CAPTURE UNIT
1 to 16
TRIGGER UNIT
- Trig type
- Counter width
- Sequencer depth
- Storage qualification
- Pipelining
- Nr of Data Groups
- Sampling clock
FIFO
- 1K to 8K depth
x widest Data Goup size
CU 1
CU 2
CU i
CU n
Sampling Clock
Cross-capture units trigger lines
(0 to n-1)
LINK
DOWNSTREAM LINK
- I2C or Transceiver link
- I2C pin location
- I2C I/O standard
- Rx# parameters if SFP is used
Std FPGA pins (2x)
or
Rx#
TRANSCEIVERS
- 1 to 4
- Tx type
- Tx bank
- Tx site
- Line rate
- Ref. clock
Tx0
Tx1
Tx2
Tx3
Transceivers reference clock

EXOSTIV LABS Visibility into the FPGA.

EXOSTIV

- 32K nodes per FPGA max
- 8 GB memory
- 50 Gbps bandwidth
- > 350 MHz operation
- Data multiplexing, triggering, filtering, event counters
- Integrated waveform viewer
- Xilinx Series 7, Ultrascale(+), Zynq / Intel Series 10 support

Thank you.