Interfacing EXOSTIV Probe EP Series

User Guide

Rev. 2.0.2 - August 29, 2017

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References

[1] SFF committee, INF-8074i specification for SFP (Small Formfactor Pluggable) Transceiver (May 12, 2001)

Revision History

Revision	Modifications
1.0.26	• Original revision
1.0.47	• Notes added below Table 2 • HDMI I²C minimum reference level changed to +2.5V. Table updated accordingly • Notes added below Table 4 • Different minimum VREF value for GPIO lines 0-3 (+1.5V) and 4-5 (+1.65V) • Pin mapping correction for GPIO connector (Figure 2 and Table 6) • DC characteristics for GPIO lines split in Table 8 and Table 9
1.0.53	• Pin mapping for HDMI type-C added (Table 2)
1.0.86	• Extended document to cover all EP devices
2.0.0	• General review with EXOSTIV Dashboard for Intel release
2.0.1	• Corrected some typos
2.0.2	• Removed description of optical SFP cables.

Interfacing EP Series

Introduction

EXOSTIV Probe ('EP Series') device requires a bi-directional link to connect to the target system. This bi-directional link is composed of:

- a low data rate downstream link from the EP device to the target system. It is used to configure and control the IP embedded in the FPGA.
- a high speed upstream link from the target FPGA to the EP device to collect the captured data.

The EP series devices use transceivers (or 'multi-gigabit transceivers', or 'MGT') to implement the upstream link. All the EP Probe devices provide 2 connection options: up to 4 SFP/SFP+ cages able to receive passive SFP copper cables or SFP/SFP+ optical transceiver modules[1] and an HDMI connector type-A with up to 4 simplex multi-gigabit links.

The low data rate downstream link is implemented using either MGT or a low speed serial link similar to I²C.

The purpose of this document is to provide the necessary information to correctly connect the EP series devices to the user's target system. Pin assignments, mechanical and electrical specifications of the connectors are provided to help designers implement interfaces compatible with Exostiv Labs devices.

The following models of EXOSTIV Probes EP series are currently available:

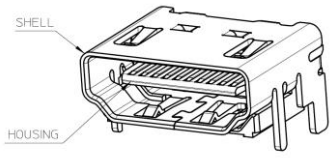
EXOSTIV Probes	**EP3000**	**EP6000**	**EP12000**
Max. speed per channel	3.75 Gbps	6.6 Gbps	12.5 Gbps
Number of channels (Transceivers)	1,2 or 4		
Supported devices	Xilinx FPGA : please click here. Intel FPGA : please click here.		

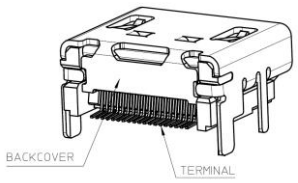
EXOSTIV Probe user's guide can be found on Exostiv Labs' general documentation page.

Notes : 1. *Please contact us for other devices and manufacturers support, availability and roadmaps.*
2. *FPGA devices that will be supported in the future with the EP3000, EP6000 and EP12000 probes will use the pinout described in this document.*
3. *Other probe number encoding such as EP6000-X, EP12000-X, EP6000-I or EP12000-I with 'X' or 'I' suffix are now covered by the generic numberings 'EP3000', 'EP6000' and 'EP12000'.*

HDMI Connector

The HDMI port is implemented using a 19-pin type-A HDMI compatible connector. Industry standard HDMI cables can be used to connect the EP devices to the user's target system. Table 1 provides some examples of compatible connectors that can be placed onto the target system board.





Even if the EP devices use a type-A HDMI connector, the target system can be equipped with space saving type-C (mini-HDMI) or type-D HDMI (micro-HDMI) connectors. In this case, a connector adapter or a cable with a different connector on each end must be used to connect the EP device to the target system. Using type-B induces the presence of via on the transceiver lines. With type-A connector, straight routing without via is possible.

[1] Although the receiving cage can be compatible with optical fiber, **EXOSTIV will NOT work with optical cables**. Copper cables must be used.

Table 1: Examples of compatible HDMI connectors

Manufacturer	Part Number	Connector Type
Molex	047151-1001	Type-A
FCI	10029449-001RLF	Type-A
TE Connectivity	1747981-1	Type-A
CNC Tech	2000-1-2-30-00-BK	Type-A
Molex	046765-0001	Type-D
CNC Tech	2002-1-2-40-30-BK	Type-D

This list is not exhaustive.

Table 2 provides the pin assignments for type-A, type-C and type-D HDMI connectors. The HDMI interface uses up to 4 simplex multi-gigabit links from the target system to the EP device (upstream data flow direction). The differential GTX data lines must be connected to the dedicated transmitter pins of the FPGA (MGTPTX, MGTXTX or MGTHTX). It is recommended to place AC coupling capacitors on the target system as close as possible to the FPGA pins.

Table 2: HDMI Type-A and Type-D connector pin assignments

Type-A[1]	Type-C[4]	Type-D[2]	Signal	Description
1	2	3	T2Y_Data3+	Positive data line of the 4th GTX[2] differential pair from target system to EP device. Connect to MGTPTXP, MGTXTXP or MGTHTXP pin of the FPGA.
2	1	4	D3_Shield	Shield for 4th GTX differential pair
3	3	5	T2Y_Data3-	Negative data line of the 4th GTX differential pair from target system to EP device. Connect to MGTPTXN, MGTXTXN or MGTHTXN pin of the FPGA.
4	5	6	T2Y_Data2+	Positive data line of the 3rd GTX differential pair from target system to EP device. Connect to MGTPTXP, MGTXTXP or MGTHTXP pin of the FPGA.
5	4	7	D2_Shield	Shield for 3rd GTX differential pair
6	6	8	T2Y_Data2-	Negative data line of the 3rd GTX differential pair from target system to EP device. Connect to MGTPTXN, MGTXTXN or MGTHTXN pin of the FPGA.
7	8	9	T2Y_Data1+	Positive data line of the 2nd GTX differential pair from target system to EP device. Connect to MGTPTXP, MGTXTXP or MGTHTXP pin of the FPGA.
8	7	10	D1_Shield	Shield for 2nd GTX differential pair
9	9	11	T2Y_Data1-	Negative data line of the 2nd GTX differential pair from target system to EP device. Connect to MGTPTXN, MGTXTXN or MGTHTXN pin of the FPGA.
10	11	12	T2Y_Data0+	Positive data line of the 1st GTX differential pair from target system to EP device. Connect to MGTPTXP, MGTXTXP or MGTHTXP pin of the FPGA.
11	10	13	D0_Shield	Shield for 1st GTX differential pair
12	12	14	T2Y_Data0-	Negative data line of the 1st GTX differential pair from target system to EP device. Connect to MGTPTXN, MGTXTXN or MGTHTXN pin of the FPGA.
13	13	15	DNC	Do not connect. Keep this pin floating.
14	14	2	DNC	Do not connect. Keep this pin floating.
15	15	17	Y2T_SCL	I²C serial clock from EP to target system. EP device is the I²C bus master. Add 2KΩ pull-up resistor on target system. Connect this pin to an FPGA user IO.
16	16	18	Y2T_SDA	I²C serial bi-directional data line. Add 2KΩ pull-up resistor on target system. Connect this pin to an FPGA user IO.
17	17	16	GND	Reference signal ground
18	18	19	DNC	Do not connect. Keep this pin floating.
19	19	1	Presence Detect	Target presence detection. Connect this pin to signal ground.

[1] *Tested with 10 m cable up to 6.6 Gbps per link and with 2 m cable up to 10.0 Gbps.*
[2] *Tested with 2 m cable up to 10.0 Gbps per link. Higher bit rates tests underway Please contact us for details.*
[3] *Transceiver + and – signals can be swapped within a differential pair if it is required to improve the layout. The EP can dynamically invert the polarity of the received signals.*
[4] *Not tested yet – provided 'as is'.*

When using the HDMI connector, the downstream communication (from the EP device to the target system) is implemented with the dedicated I²C serial bus of the HDMI connector. This link is used to control the IP that is embedded in the FPGA fabric. The EP device operates as the bus master and the target system as the slave. SCL and SDA lines must be connected to user IO pins of the FPGA; in addition, external pull-up resistors connecting SCL and SDA to a voltage reference from +2.5V to +3.3V must be added. If this voltage level range is not compatible

[2] GTX = 'Gigabit transceiver' or 'transceiver'. The abbreviation can change according to the FPGA vendor and FPGA family. In this document 'GTX' is used as a generic term.

with the selected FPGA bank, an I²C bus level converter must be inserted between the HDMI connector and the FPGA.

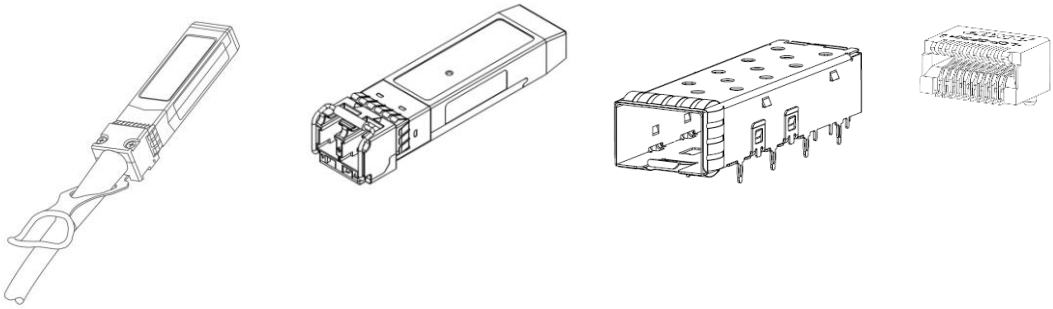
Table 3: I²C bus specifications through HDMI connector

Parameter		Min	Typ	Max	Unit
Voltage reference	V_{REF}	2.5V	-	3.3V	V
SCL/SDA pull-up resistor	-	-	2	-	kΩ
SCL/SDA voltage level (input to EP)					
Low-level	V_{IL}	-0.5	-	0.85	V
High-level	V_{IH}	2.31	-	6	V
Low-level output current	I_{OL}	3	9	-	mA

Note: *Even if an industry standard HDMI connector is used on EP series, do not connect any HDMI-compatible device. The multi-gigabit transceiver port **is not** pin and functionality-compatible with the HDMI video standard.*

SFP/SFP+ Cages

EP series can be connected to up to 4 simplex or full-duplex multi-gigabit links through SFP/SPF+ physical interface. The SFP/SFP+ cages can receive passive cables. Exostiv will not work with optical cables. The connector pin assignment is compatible with the standard proposed by the MSA group [1].



Using the SFP/SFP+ interface enables the implementation of a full-duplex link. Upstream data flow (TX) refers to data transmitted from the target system to the EP device. Downstream data flow (RX) refers to data received by the target system from the EP device.

A downstream link is mandatory to let the EP device control the IP embedded in the FPGA. A single downstream link is required, even if multiple SFP/SFP+ links are used for the upstream link.

This downstream link does not need to be implemented using a multi-gigabit link since only a very low data rate is required in this direction.

When the downstream link does not use the multi-gigabit transceiver, it must be implemented with a I²C bus. Two user IO pins of the FPGA must be reserved to connect the SCL and SDA lines of the I²C interface. Refer to 'HDMI Connector' section for more details on how to implement the I²C interface.

Figure 1: SFP+ receptacle pin mapping

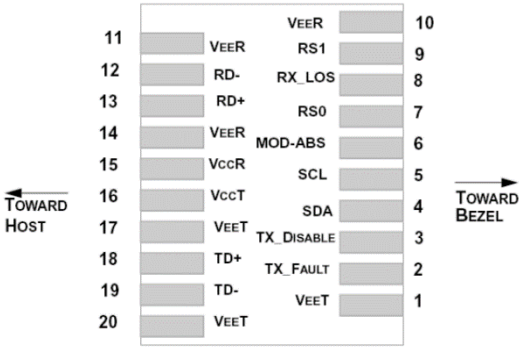


Table 4: SFP/SFP+ connector pin assignment

Pin #	Signal	Description	Usage
1	VeeT	Transmitter ground	Mandatory
2	TX Fault	Transmitter fault indication. Open collector/drain output. 4.7K to 10K pull-up required.	Optional
3	TX Disable	Active high transmitter disable.	Optional
4	MOD-DEF2	SDA line for I²C interface. Pull-up resistor required.	Optional
5	MOD_DEF1	SCL line for I²C interface. Pull-up resistor required.	Optional
6	MOD-DEF0	Active low module presence detection. Pull-up resistor required.	Optional
7	RS0	Receiver rate select.	Optional
8	LOS	Loss of receiver signal. Open collector/drain output. 4.7K to 10K pull-up required.	Optional
9	RS1	Transmitter rate select.	Optional
10	VeeR	Receiver ground	Mandatory
11	VeeR	Receiver ground	Mandatory
12	RD-	Inverted received data out. Connect to MGTPRXN, MGTXRXN or MGTHRXN pin of the FPGA.	Optional[1]
13	RD+	Received data out. Connect to MGTPRXP, MGTXRXP or MGTHRXP pin of the FPGA.	Optional[1]
14	VeeR	Receiver ground.	Mandatory
15	VccR	Receiver power.	Optional[2]
16	VccT	Transmitter power.	Mandatory[3]
17	VeeT	Transmitter ground.	Mandatory
18	TD+	Transmit data in. Connect to MGTPTXP, MGTXTXP or MGTHTXP pin of the FPGA.	Mandatory
19	TD-	Inverted transmit data in. Connect to MGTPTXN, MGTXTXN or MGTHTXN pin of the FPGA.	Mandatory
20	VeeT	Transmitter ground	Mandatory

[1] *Optional if downstream link is implemented using I²C bus*
[2] *Not required if RD+/RD- are not used. Optional if only passive cables are used for RD+/RD-*
[3] *Optional if only passive cables are used for TD+/TD-*
[4] *Transceiver + and – signals can be swapped within a differential pair if it is required to improve the layout. The EP can dynamically invert the polarity of the received signals.*

When passive cables are used, it is not mandatory to provide power on these pins and they can be connected to GND. Please note that the internal identification EEPROM cannot be accessed if no power is provided to the SFP cable. In this case, the cable will operate correctly but the diagnostic features won't be available.

TD+/TD- are mandatory and are used for the upstream link to the EP device. This differential pair must be connected to the dedicated transmitter pins of the FPGA (MGTPTX, MGTXTX or MGTHTX). It is recommended to place AC coupling capacitors on the target system as close as possible to the FPGA pins.
RD+/RD- are not mandatory. They can be used for the downstream link from the EP device.

If multiple SFP/SFP+ links are used, a single downstream link is required. If no SFP/SFP+ link is used for downstream link, an I²C bus interface must be foreseen. Refer to "HDMI Connector" section for more details. The *RD+/RD-* differential pair must be connected to the dedicated receiver pins of the FPGA (MGTPRX, MGTXRX or MGTHRX). AC coupling capacitors are placed in the EP devices for the downstream links and hence no AC coupling capacitor is required for the receiver lines on the target system.

The control and status signals of the SPF/SFP+ connector are not mandatory. Connecting these pins to an FPGA bank compatible with +3.3V IO signalling allows using the diagnostic features of the IP embedded in the target FPGA. These pins are not required for the IP operation. Table 5 describes how to connect these pins if the diagnostic feature is not used. The IP diagnostic feature gives the possibility to automatically detect the module or cable presence, to read the module or the cable identification, and so on.

If multiple SFP/SFP+ links are used, it is possible to spare FPGA pins by connecting the corresponding control and status lines of modules together.

Note: 

The I²C bus of multiple SFP/SFP+ links cannot be connected together to form a single bus. All modules have the same I²C slave address. Placing several modules on the same bus will create conflicts. One I²C (SDA/SCL) pair must be used per SFP/SFP+ links. An I²C bus switch component can be added on board to reduce the number of used FPGA user IO.

Table 5: Handling unused SFP/SFP+ control and status signals.

Pin #	Signal	Description
2	TX Fault	Keep unconnected when not used.
3	TX Disable	Must be connected to GND to enable the module by default.
4	MOD-DEF2	Pull-up to +3.3V.
5	MOD_DEF1	Pull-up to +3.3V.
6	MOD-DEF0	Keep unconnected when not used
7	RS0	This pin has no effect for passive cables. Pull-up resistor of maximum 10K is recommended (check optical module manufacturer documents for more details).
8	LOS	Keep unconnected if not used.
9	RS1	This pin has no effect for passive cables. Pull-up resistor of maximum 10K is recommended (check optical module manufacturer documents for more details).

GPIO Interface

(Reserved for future use. Please contact Exostiv Labs to check about GPIO Interface availability & activation).

If the downstream channel from the EP device to the target system is not implemented through the HDMI connector or through an SPF/SFP+ link, then the GPIO connector must be used.

Not all EP series devices provide the *General Purpose Input-Output* (GPIO) connector. Please refer to the devices documentation for more details. When the GPIO connector is not present, the downstream link must be implemented using one of the two high data rate interfaces (HDMI or SFP/SFP+).

The GPIO interface is designed to implement the following serial protocols:

- I²C : low speed protocol using reduced amount of user IO on the target FPGA.
- SPI : faster serial interface using a minimum of 3 user IO on the target FPGA.
- JTAG: low speed protocol using only dedicated FPGA pins.

By default, when the IP is generated with the GPIO as downstream link, the I²C protocol is selected. Refer to Figure 2 and Table 6 for pin assignments. For proper operation, the user must provide a valid DC reference voltage through pin 2. The reference voltage is required no matter the selected operating mode. The GPIO interface operates for any voltages between +1.5V(2) and +3.3V. Table 8 and Table 9 Table provide the DC characteristics for the GPIO interface. GPIO lines must be connected to user IO of the target FPGA within a bank having VccO voltage corresponding to the provided V_{REF} level. GPIO lines that are not used for the selected serial protocol can be left floating (not connected to the FPGA). Do not connect unused GPIO lines to GND or any other DC voltage.

Notes: 1. ***Currently, only I²C is available.*** *SPI and JTAG will be available in the future releases (please contact us for roadmaps) of the EP devices. The pin assignment is described in Table 6 to let the user build up an interface compatible with upcoming features.*

2. *V_{REF} can be as low as +1.5V for GPIO lines 0 to 4. For GPIO lines 5 and 6 the minimum reference voltage is limited to +1.65V.*

Figure 2: GPIO male header pin mapping

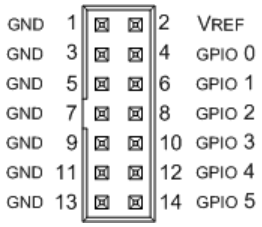


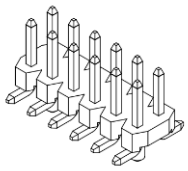
Table 6: GPIO connector pin assignment vs operating mode.

Pin #	GPIO	I²C	SPI(2)	JTAG(2)
2	V_{REF}	V_{REF}	V_{REF}	V_{REF}
4	GPIO 0	-	SSn[1]	TMS
6	GPIO 1	-	SCLK	TCK
8	GPIO 2	-	MISO	TDO
10	GPIO 3	-	MOSI	TDI
12	GPIO 4	SCL	-	-
14	GPIO 5	SDA	-	-
1, 3, 5, 7, 9, 11, 13	GND	GND	GND	GND

[1] *The SPI slave select pin is optional and is reserved for future use.*

[2] *SPI and JTAG will be available in future releases (please contact us for roadmaps)*

The GPIO connector is a 14-pin dual row shrouded header with a pitch of 2.0 mm. The EP devices offering this interface are provided with a flat cable having female connector on both ends. Table 7 provides some examples of mating header connectors.



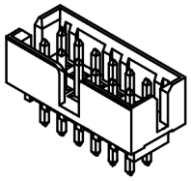


Table 7: Examples of mating pin header

Manufacturer	Part Number	Connector Type
Molex	087833-1420	Dual row, 14-pin shrouded header, right angle, through hole.
Molex	087831-1420	Dual row, 14-pin shrouded header, vertical, through hole
FCI	98424-G52-14ALF	Dual row, 14-pin shrouded header, vertical, surface mount
3M	951214-2520-AR-PR	Dual row, 14-pin unshrouded header, vertical, surface mount

This list is provided is not exhaustive.

Table 8: GPIO absolute maximum ratings

Parameter		Min	Max	Unit
Reference voltage	V_{REF}	-	6	V
Reference supply current	$I_{cc,max}$	-	100	mA
GPIO line DC current	I_{OUT}	-	±12	mA

Table 9: Recommended DC characteristics for GPIO0, GPIO1, GPIO2 and GPIO3

Parameter		Min	Max	Unit
Reference voltage	V_{REF}	1.5	3.3	V
High level output voltage				
V_{REF}=3.3V; I_{OH}=-8mA	V_{OH}	2.25		V
V_{REF}=2.5V; I_{OH}=-8mA		2.15		
V_{REF}=1.8V; I_{OH}=-8mA		1.55		
V_{REF}=1.5V; I_{OH}=-8mA		1.30		
Low level output voltage				
V_{REF}=3.3V; I_{OH}=8mA	V_{OL}		0.40	V
V_{REF}=2.5V; I_{OH}=8mA			0.30	
V_{REF}=1.8V; I_{OH}=4mA			0.26	
V_{REF}=1.5V; I_{OH}=4mA			0.24	
High-level input voltage				
V_{REF} = 1.5V to 3.3V	V_{IH}	1.35		V
Low level input voltage				
V_{REF} = 1.5V to 3.3V	V_{IL}		0.45	V

Table 10: Recommended DC characteristics for GPIO4 and GPIO5 (I^2C)

Parameter		Min	Max	Unit
Reference voltage	V_{REF}	1.65	3.6	V
High level output voltage V_{REF}=1.65V to 3.6V; I_{OH}=-1mA	V_{OH}	0.67 x V_{REF}		V
Low level output voltage V_{REF}=3.3V; I_{OH}=1mA	V_{OL}		0.40	V
High-level input voltage V_{REF}=1.65V to 1.95V V_{REF}=2.3V to 3.6V	V_{IH}	V_{REF}-0.2 V_{REF}-0.4		V
Low level input voltage V_{REF} = 1.65V to 3.6V	V_{IL}		0.15	V

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