EXOSTIV Probe and Blade IPs

User's Guide

Rev. 1.0.0 - September 9, 2024

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References

Revision History

Revision	Modifications
1.0.0	• Initial revision

EXOSTIV Probe and Blade IPs

Introduction

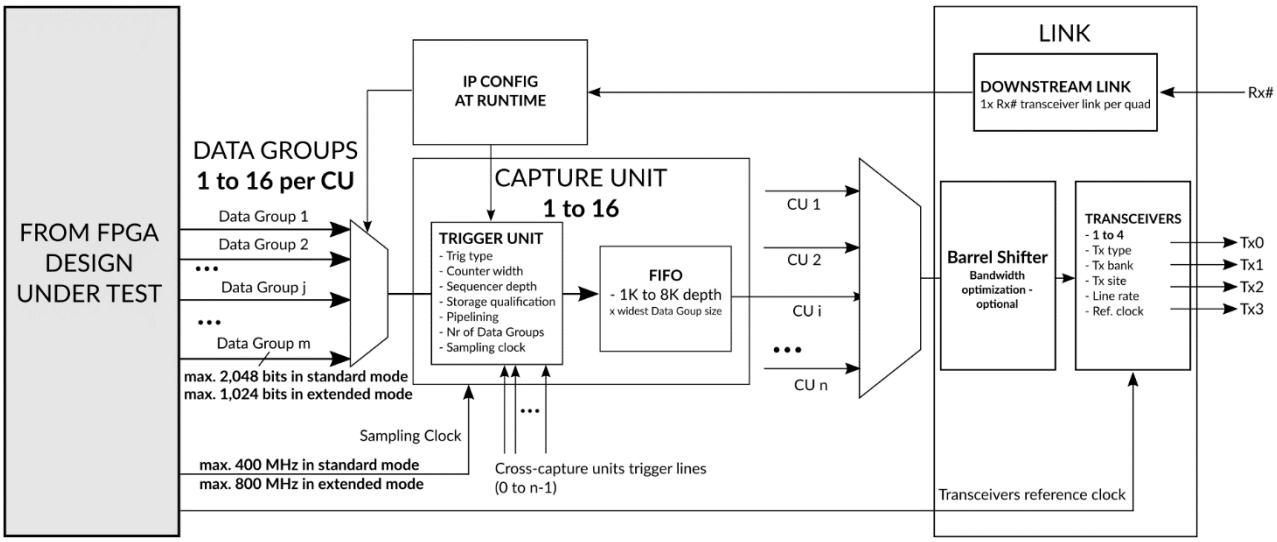
From software environment v2 (DARK), the same architectures of IPs are generated for EP16000 probe and Exostiv Blade Series. The present guide is dedicated to the description of the available IPs for these devices and the provided configuration options.

The IPs provided for use with Exostiv Probe 'EP16000' type and Exostiv Blade are currently available for AMD FPGA and Programmable Devices only.

'EXOSTIV IP' is a configurable IP block that is configured and inserted into a target FPGA from EXOSTIV Dashboard. It aims at reaching and capturing the evolution over time of internal FPGA signals (FPGA 'nodes').

Overview

Figure 1: Standard IP general view



Features

- Configurable upstream link, using 1 to 4 FPGA transceivers up to 28.125 Gbps[1]
- Downstream link to configure IP at run-time, without the need to re-implement instrumented design.
- From 1 to 16 configurable 'Capture Units' (CU) to sample FPGA internal nodes, with trigger and data qualification resources and selectable FIFO size.
- From 1 to 16 multiplexed Data Groups per CU, selectable at run time through downstream link.
- From 16 to 2,048 bits per Data Group, connected to the target FPGA internal nodes.
- Configurable clock signal for each capture unit, enabling multiple clock domains capture.
- Cross-CU trigger lines

[1] Target FPGA-dependent. The ability to capture at the chosen speed depends on the Exostiv Labs hardware used. EP16000 is limited to 16.25 Gbps per transceiver; Exostiv Blade series support 28.135 Gbps transceivers.

Link Configuration

The 'link' implements the connection with the used Exostiv Labs hardware. It is composed of 2 parts:

- The 'Transceivers' (or 'SERDES') that uses up to 4 FPGA transceivers. This resource is automatically shared by all the IP's Capture Units – refer to section 'Capture Configuration'.
- The 'Downstream Link', that is used at runtime to change the IP settings at runtime (e.g.: the configuration of the multiplexers used to select the observed Data Groups).

The link is configured with the Exostiv Core Inserter 'link configuration' screen.

Figure 2: Standard IP link configuration in Exostiv Core Inserter software.

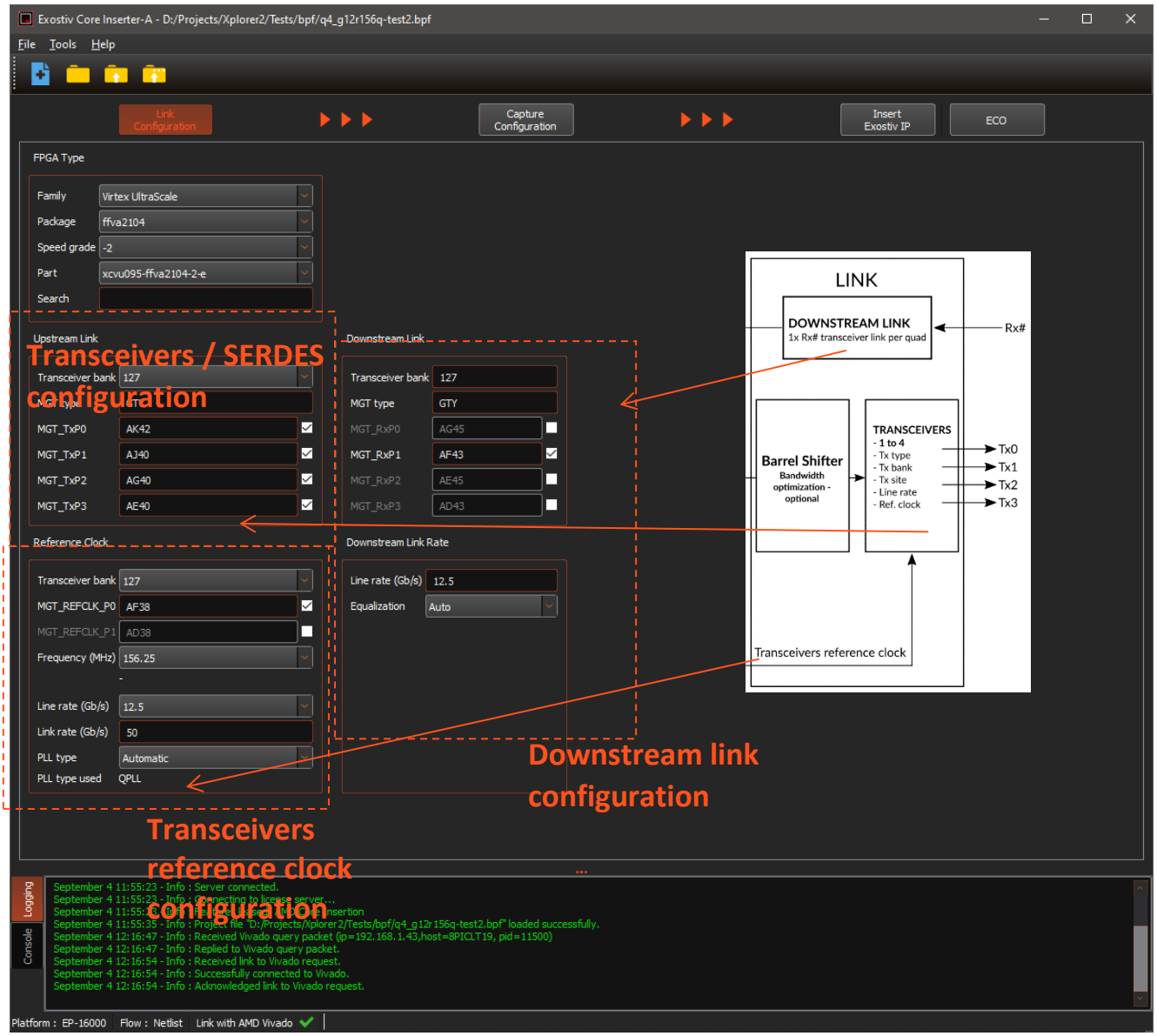


Table 1: FPGA Type parameters

Parameter	Description	Status and limitations
Family	Use dropdown box to select the target FPGA family.	**Supported families:** AMD devices – see on this page for an updated list.
Package	Use dropdown box to select the target FPGA package.	-
Speed grade	Use dropdown box to select the target FPGA speed grade.	-
Part	Use dropdown box to select the target FPGA part.	-

Table 2: Upstream link parameters

Parameter	Description	Status and limitations
Transceiver bank	Use dropdown box to select the target FPGA bank of the transceivers used for EXOSTIV	**Check Note 'Upstream link implementation constraints' under this table.**
MGT Type	Informative, depends on the selected FPGA	
MGT_TxP0	Informative, shows the location of TxP0 in the selected transceiver bank. Select tick box to enable this transceiver with EXOSTIV.	
MGT_TxP1	Informative, shows the location of TxP1 in the selected transceiver bank. Select tick box to enable this transceiver with EXOSTIV.	
MGT_TxP2	Informative, shows the location of TxP2 in the selected transceiver bank. Select tick box to enable this transceiver with EXOSTIV.	
MGT_TxP3	Informative, shows the location of TxP3 in the selected transceiver bank. Select tick box to enable this transceiver with EXOSTIV.	

Note: ***Upstream link implementation constraints:***

1) *All transceiver channels must be in the same bank and quad.*
2) *For each transceiver channel, the full differential pair (Tx and Rx) must be available.*
3) *Using the transceivers requires reserving a PLL resource from the channel. The requested line rate defines whether a CPLL can be used or if a QPLL must be used. The choice of the CPLL or the QPLL depends on the FPGA family, the chosen data rate and the frequency of the transceivers reference clock. This choice is made either automatically by the EXOSTIV Core Inserter interface when setting up the EXOSTIV IP link or manually.*

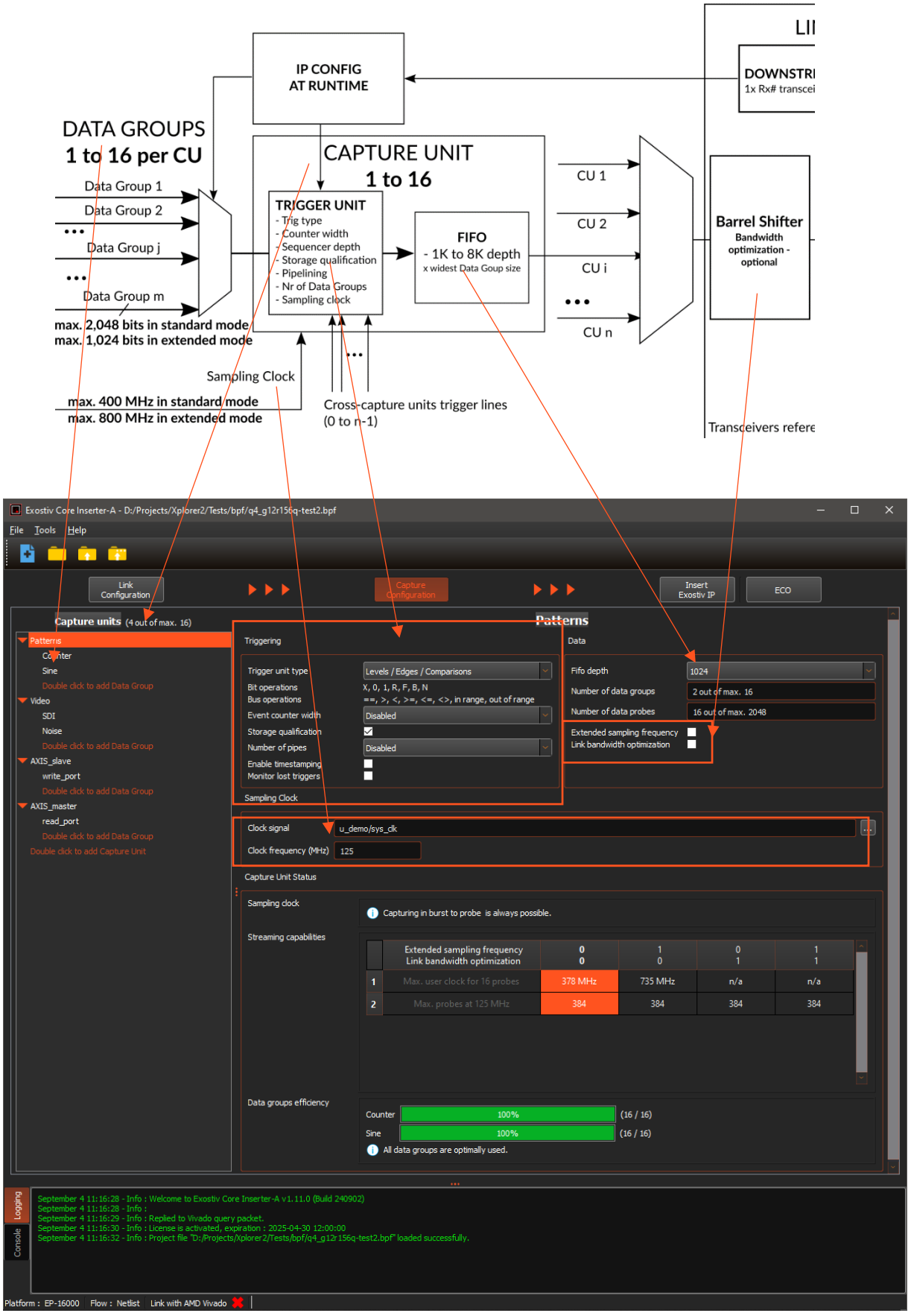
Table 3: Reference Clock parameters

Parameter	Description	Status and limitations
Transceiver bank	Use dropdown box to select the transceiver bank from which the clock of the transceiver should be taken.	Refer to implementation constraints and DC & Switching characteristics of the target FPGA.
MGT_REFCLK_P0	Available reference clock selection. Use tick box to use this reference clock.	
MGT_REFCLK_P1	Available reference clock selection. Use tick box to use this reference clock.	
Frequency (MHz)	Use drop down list to specify the frequency of the transceivers reference clock picked from the FPGA under test. If you cannot find the desired frequency, please contact Exostiv Labs support.	
Line rate (Gb/s)	Use drop down list to select the transceivers' line rate in Gbit per second. The available choices are derived from the specified reference clock frequency.	
Link rate (Gb/s)	Informative: shows the total available bandwidth when using the selected transceivers at the specified line rate.	

Downstream Link parameters		
Transceiver bank	Specifies the transceiver bank in which the downstream link is implemented.	
MGT_RxP0	Informative, shows the RxP0 pin location in the selected bank of the selected FPGA. Select the tick box to use it for the downstream link.	Only one of the transceivers has to be selected for the downstream link.
MGT_RxP1	Informative, shows the RxP1 pin location in the selected bank of the selected FPGA. Select the tick box to use it for the downstream link.	
MGT_RxP2	Informative, shows the RxP2 pin location in the selected bank of the selected FPGA. Select the tick box to use it for the downstream link.	
MGT_RxP3	Informative, shows the RxP3 pin location in the selected bank of the selected FPGA. Select the tick box to use it for the downstream link.	

Capture Configuration

Figure 3: EXOSTIV IP Capture configuration in EXOSTIV Dashboard



The ‘Capture Configuration’ window is used to define the Capture Units and their characteristics.
The window’s contents change according to the context. It is divided in 2 main panes:

- A column on the left side of the window provides an overview of the defined Capture Unites and their data groups.
- The main content window changes when a specific capture unit or a related data group is selected from the left side column.

Figure 3 shows the contents of the window when a Capture Unit (‘Capture Unit 1’) is selected. **Figure 4** shows the contents of the window when a data group (‘Sine’ data group of ‘Capture Unit 1’) is selected.

Figure 4: EXOSTIV Standard IP Capture configuration – Data group options

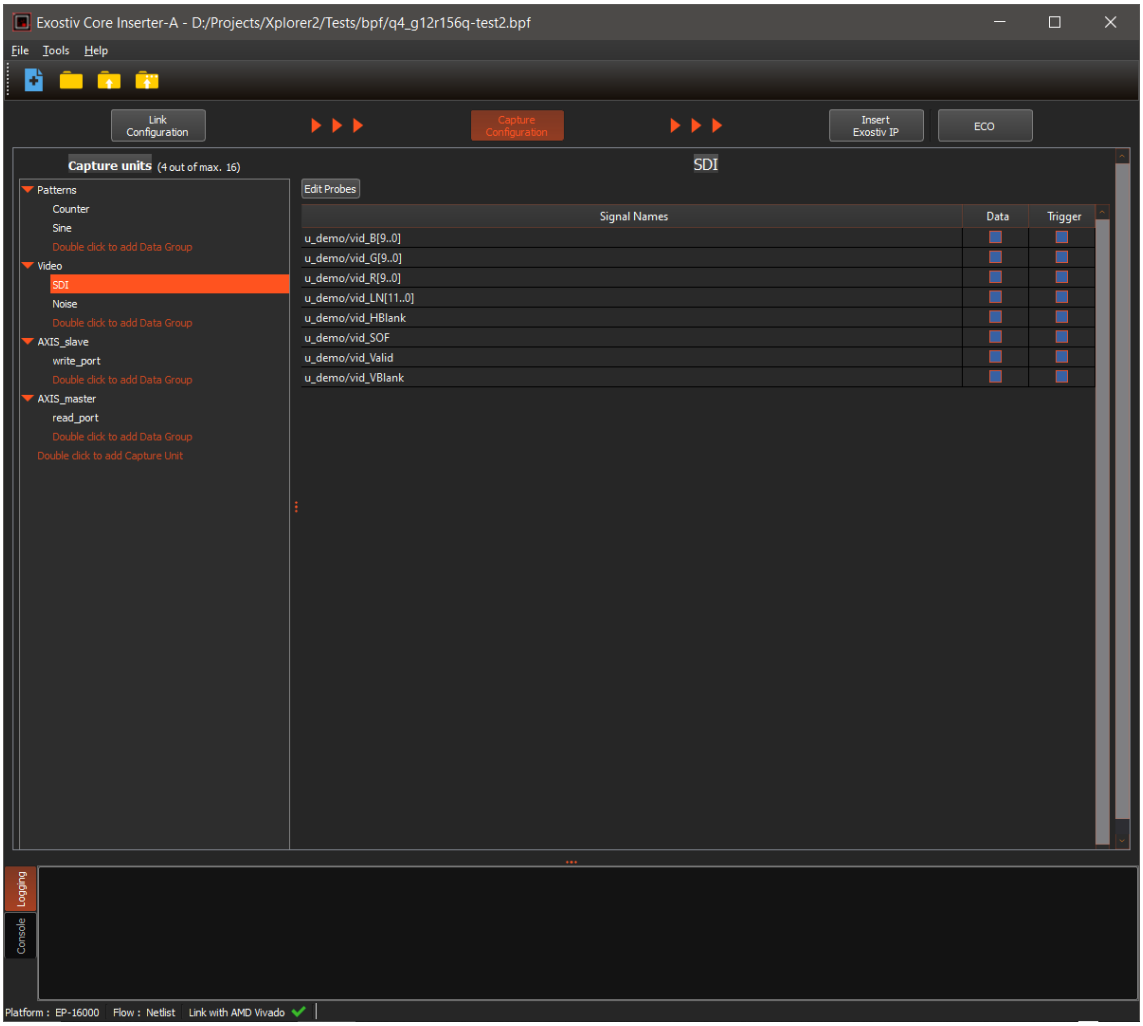


Table 4: Triggering parameters (refer to Figure 3)

Parameter	Description	Status and limitations
Trigger unit type	Use dropdown box to select between: 'Levels / Edges / Comparisons' 'Level /Edges'	Disabling comparisons saves on the logic needed to implement the capture units but does not allow triggering capture on inequalities or value ranges for bus operations.
Bit operations	Informative: shows the types of arguments that can be used for the triggering conditions at bit level. X : don't care 0 : logic 0 1 : logic 1 R : Rising edge F : Falling edge B : Both edges N : No edge / No transition	
Bus operations	Informative: shows the types of arguments that can be used for the triggering conditions at bit level. == : equality > : greater than < : smaller than >= : greater than or equal to <= : smaller than or equal to in range : trigger when inside the specified value range out of range : trigger when outside the specified value range	
Counter width	Use dropdown box to specify the width in number of bits of an event counter for the trigger. Legal values: Disabled, or 1 to 32 bits.	
Storage qualification	Select tick box to enable 'storage qualification conditions' at runtime. Storage qualification enables filtering captured data according to a logic condition defined on it (e.g., only capture data if a 'data enable' signal is active).	
Number of pipes	Use drop down box to enable and insert pipelining in the data path of this capture unit. Up to 8 stages can be added for each data group before the data group selection multiplexer.	
Enable timestamping	When selected, this tick box enables the timestamp generator in the IP	In roadmap. Will be available in future versions.
Monitor lost trigger	When selected, enables reporting potentially lost trigger events, due to capture characteristics.	In roadmap. Will be available in future versions.

Table 5: Data parameters (refer to Figure 3)

Parameter	Description	Status and limitations
Fifo[1] Depth	Use dropdown to select the Capture Unit's Fifo depth. Values can be chosen between 1,024 – 2,048 – 4,096 – 8,192	The Fifo is used as a temporary buffer to accommodate for different clock rates at the input of EXOSTIV IP and at the transceivers level. The Fifo size also defines the maximum burst size in 'Burst Mode' when capturing data.
Number of data groups	Informative: reports or defines the number of data groups for the currently selected capture unit.	Using more than one data groups inserts a multiplexer at the input of the capture unit. This multiplexer can be switched at runtime to enable observation of a reduced set of data and save on the transceivers' bandwidth.
Number of data probes	Informative in netlist mode of insertion, editable in RTL mode of insertion: reports or defines the number of input bits to the selected capture unit.	
Number of data only probes	Only in RTL mode of operation: defines the number of probes that cannot be used as a trigger.	Helps reduce the complexity of the capture unit.

[1] *The Fifo width is automatically selected as the size of the widest of the connected Data Groups.*

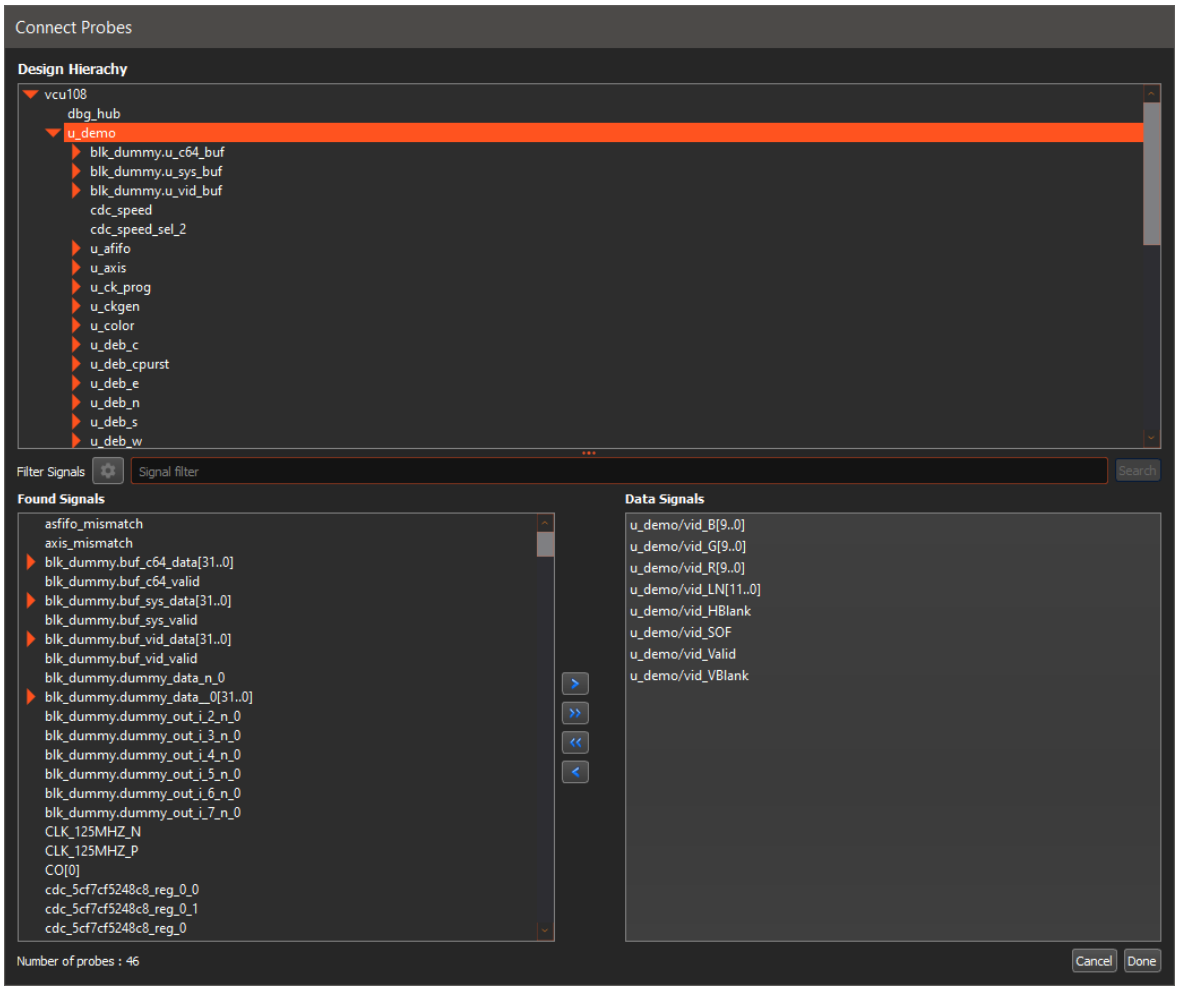
Table 6: Sampling Clock (refer to Figure 3) ***(netlist flow only)***

Parameter	Description
Clock signal	This this edit box to specify the clock signal from the FPGA design under test, that has to be used as a sampling clock for the specified connected nodes. Click on the '…' button to open a dialog and select the clock signal from the loaded target design.
Clock Frequency (MHz)	In this field, the sampling clock frequency for the chosen capture unit must be specified in MHz.

Table 7: Data groups parameters (refer to Figure 4)

Description
The main window shows the list of the FPGA nodes selected for the active Data Group. Select the 'Data' and 'Trigger' tick box to enable using the corresponding nodes as 'data only' or as 'data AND trigger'. If a signal is selected as a 'trigger', a trigger condition can be defined on it at runtime to capture data. In **netlist flow only,** clicking on the **'Edit Probes'** button opens a dialog box to select the list of signals from the loaded target design (refer to Exostiv Dashboard user's guide). In **RTL flow,** it is not allowed to connect the probes from the Dashboard interface, as this has to be done 'manually' by the user at RTL level. The 'connections' are simply the result of instantiating and connecting EXOSTIV IP from inside the RTL code.

Figure 5: Capture Unit probes connection dialog box



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